

AMIS-30532

Micro-Stepping Motor Driver

Introduction

The AMIS-30532 is a micro-stepping stepper motor driver for bipolar stepper motors. The chip is connected through I/O pins and an SPI interface with an external microcontroller. It has an on-chip voltage regulator, reset-output and watchdog reset, able to supply peripheral devices. The AMIS-30532 contains a current-translation table and takes the next micro-step depending on the clock signal on the “NXT” input pin and the status of the “DIR” (=direction) register or input pin. The chip provides a so-called “speed and load angle” output. This allows the creation of stall detection algorithms and control loops based on load-angle to adjust torque and speed. It is using a proprietary PWM algorithm for reliable current control.

The AMIS-30532 is implemented in I2T100 technology, enabling both high-voltage analog circuitry and digital functionality on the same chip. The chip is fully compatible with the automotive voltage requirements.

The AMIS-30532 is ideally suited for general-purpose stepper motor applications in the automotive, industrial, medical, and marine environment. With the on-chip voltage regulator it further reduces the BOM for mechatronic stepper applications.

Key Features

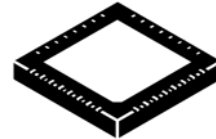
- Dual H-Bridge for 2-Phase Stepper Motors
- Programmable Peak-Current up to 1.6 A Continuous[†] (3.0 A Short Time) using a 5-bit Current DAC
- On-Chip Current Translator
- SPI Interface
- Speed and Load Angle Output
- Seven Step Modes from Full-Step Up to 32 Micro-Steps
- Fully Integrated Current-Sense
- PWM Current Control with Automatic Selection of Fast and Slow Decay
- Low EMC PWM with Selectable Voltage Slopes
- Active Fly-Back Diodes
- Full Output Protection and Diagnosis
- Thermal Warning and Shutdown
- Compatible with 5 V and 3.3 V Microcontrollers
- Integrated 5 V Regulator to Supply External Microcontroller
- Integrated Reset Function to Reset External Microcontroller
- Integrated Watchdog Function
- These Devices are Pb-Free and are RoHS Compliant*

[†]Output current level may be limited by ambient temperature and heat sinking.
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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NQFP-32, 7x7
CASE 560AA

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Designator
CCCCC = Country of Assembly

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 27 of this data sheet.

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Block DIAGRAM

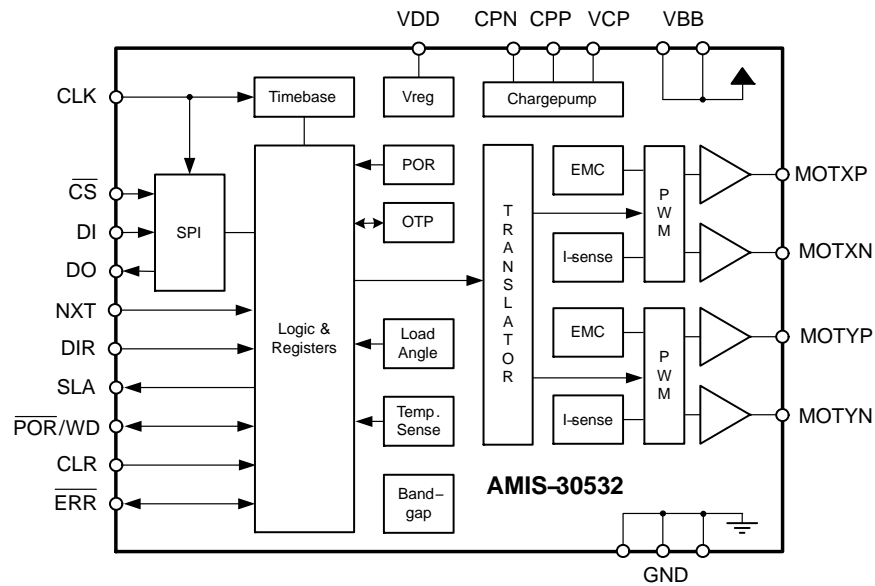


Figure 1. Block Diagram AMIS-30532

Table 1. PIN LIST AND DESCRIPTION

| Name | Pin | Description | Type | Equivalent Schematic |
|--------|--------|---|----------------|----------------------|
| GND | 1 | Ground | Supply | |
| DI | 2 | SPI Data In | Digital Input | Type 2 |
| CLK | 3 | SPI Clock Input | Digital Input | Type 2 |
| NXT | 4 | Next Micro-Step Input | Digital Input | Type 2 |
| DIR | 5 | Direction Input | Digital Input | Type 2 |
| ERR | 6 | Error Output (Open Drain) | Digital Output | Type 4 |
| SLA | 7 | Speed Load Angle Output | Analog Output | Type 5 |
| / | 8 | No Function (to be left open in normal operation) | | |
| CPN | 9 | Negative Connection of Charge Pump Capacitor | High Voltage | |
| CPP | 10 | Positive Connection of Charge Pump Capacitor | High Voltage | |
| VCP | 11 | Charge-Pump Filter-Capacitor | High Voltage | |
| CLR | 12 | "Clear" = Chip Reset Input | Digital Input | Type 1 |
| CS | 13 | SPI Chip Select Input | Digital Input | Type 2 |
| VBB | 14 | High Voltage Supply Input | Supply | Type 3 |
| MOTYP | 15, 16 | Negative End of Phase Y Coil Output | Driver Output | |
| GND | 17, 18 | Ground, Heat Sink | Supply | |
| MOTYN | 19, 20 | Positive End of Phase Y Coil Output | Driver Output | |
| MOTXN | 21, 22 | Positive End of Phase X Coil Output | Driver Output | |
| GND | 23, 24 | Ground, Heat Sink | Supply | |
| MOTXP | 25, 26 | Negative End of Phase X Coil Output | Driver Output | |
| VBB | 27 | High Voltage Supply Input | Supply | Type 3 |
| / | 30 | No Function (to be left open in normal operation) | | |
| POR/WD | 28 | Power-On-Reset and Watchdog Reset Output (Open Drain) | Digital Output | Type 2 |
| TST0 | 29 | Test Pin Input (to be tied to ground in normal operation) | Digital Input | |
| DO | 31 | SPI Data Output (Open Drain) | Digital Output | Type 4 |
| VDD | 32 | Logic Supply Output (needs external decoupling capacitor) | Supply | Type 6 |

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PIN DESCRIPTION

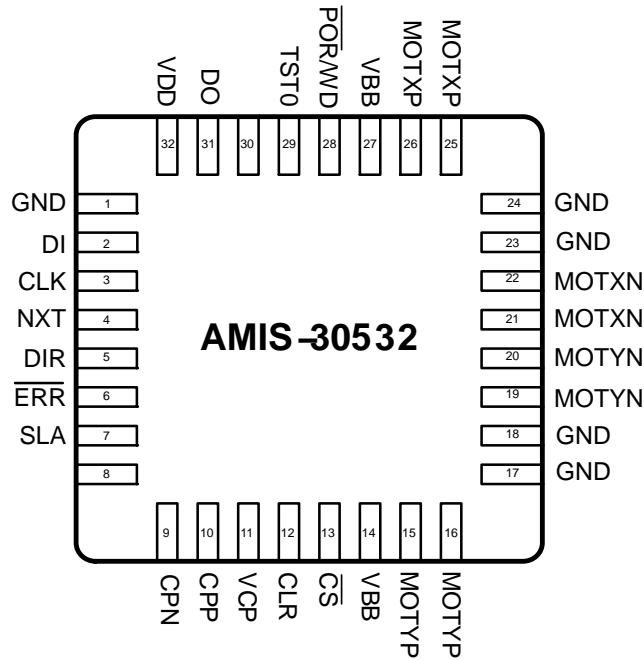


Figure 2. Pin Out AMIS-30532

Table 2. ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Min | Max | Unit |
|-----------|--|------|------|------|
| V_{BB} | Analog DC Supply Voltage (Note 1) | -0.3 | +40 | V |
| T_{ST} | Storage Temperature | -55 | +160 | °C |
| T_J | Junction Temperature under bias (Note 2) | -50 | +175 | °C |
| V_{ESD} | Electrostatic discharges on component level, All pins (Note 3) | -2 | +2 | kV |
| V_{ESD} | Electrostatic discharges on component level, HiV pins (Note 4) | -8 | +8 | kV |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. For limited time < 0.5 s.
2. Circuit functionality not guaranteed.
3. Human Body Model (100 pF via 1.5 k Ω , according to JEDEC EIA-JESD22-A114-B).
4. HiV = High Voltage Pins MOTxx, V_{BB} , GND; (100 pF via 1.5 k Ω , according to JEDEC EIA-JESD22-A114-B).

Table 3. THERMAL RESISTANCE

| Package | Thermal resistance | | | Unit |
|---------|-----------------------------|-------------------------|------------|------|
| | Junction – to – Exposed Pad | Junction – to – Ambient | | |
| | | 1S0P board | 2S2P board | |
| NQFP-32 | 0,95 | 60 | 30 | K/W |

EQUIVALENT SCHEMATICS

Following figure gives the equivalent schematics of the user relevant inputs and outputs. The diagrams are simplified representations of the circuits used.

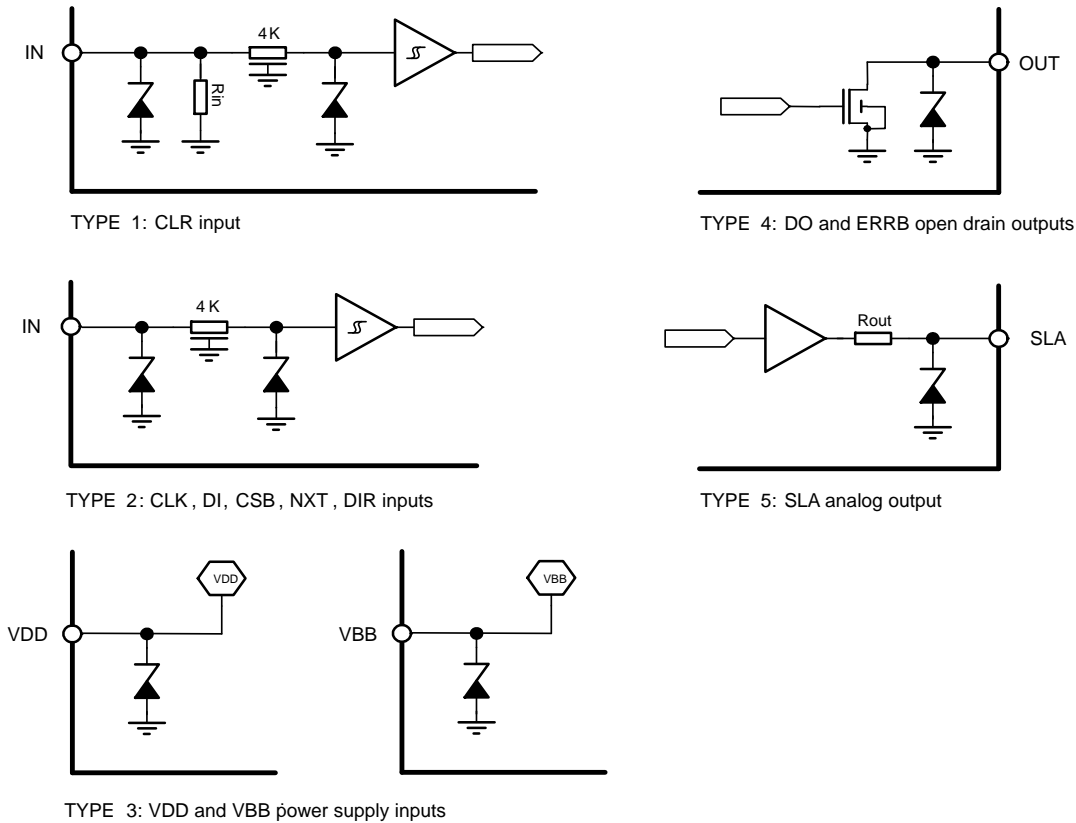


Figure 3. In- and Output Equivalent Diagram

PACKAGE THERMAL CHARACTERISTICS

The AMIS-30532 is available in a NQFP32 package. For cooling optimizations, the NQFP has an exposed thermal pad which has to be soldered to the PCB ground plane. The ground plane needs thermal vias to conduct the heat to the bottom layer. Figure 3 gives an example for good power distribution solutions.

For precise thermal cooling calculations the major thermal resistances of the device are given. The thermal media to which the power of the devices has to be given are:

- Static environmental air (via the case)
- PCB board copper area (via the exposed pad)

The thermal resistances are presented in Table 5: DC Parameters.

The major thermal resistances of the device are the Rth from the junction to the ambient (Rthja) and the overall Rth from the junction to exposed pad (Rthjp). In Table 5 below one can find the values for the Rthja and Rthjp, simulated according to JESD-51:

The Rthja for 2S2P is simulated conform JEDEC JESD-51 as follows:

- A 4-layer printed circuit board with inner power planes and outer (top and bottom) signal layers is used
- Board thickness is 1.46 mm (FR4 PCB material)
- The 2 signal layers: 70 μm thick copper with an area of 5500 mm² copper and 20% conductivity
- The 2 power internal planes: 36 μm thick copper with an area of 5500 mm² copper and 90% conductivity

The Rthja for 1S0P is simulated conform to JEDEC JESD-51 as follows:

- A 1-layer printed circuit board with only 1 layer
- Board thickness is 1.46 mm (FR4 PCB material)
- The layer has a thickness of 70 μm copper with an area of 5500 mm² copper and 20% conductivity

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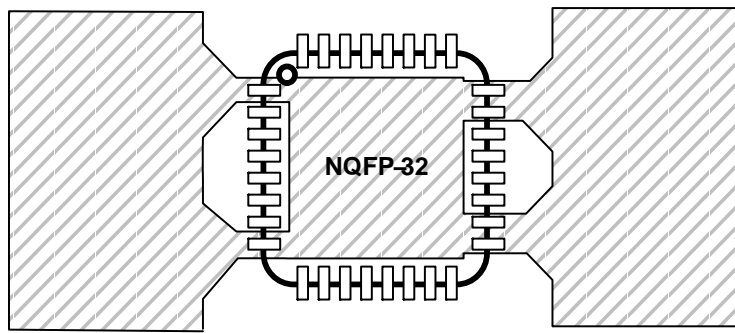


Figure 4. Example of NQFP-32 PCB Ground Plane Layout in Top View (Preferred Layout at Top and Bottom)

ELECTRICAL SPECIFICATION

Recommend Operation Conditions

Operating ranges define the limits for functional operation and parametric characteristics of the device. Note that the functionality of the chip outside these operating

ranges is not guaranteed. Operating outside the recommended operating ranges for extended periods of time may affect device reliability.

Table 4. OPERATING RANGES

| Symbol | Parameter | Min | Max | Unit |
|----------|-------------------------------|-----|------|------|
| V_{BB} | Analog DC Supply | +6 | +30 | V |
| T_J | Junction Temperature (Note 5) | -40 | +172 | °C |

5. No more than 100 cumulative hours in life time above T_{tw} .

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Table 5. DC PARAMETERS (The DC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise specified) Convention: currents flowing in the circuit are defined as positive.

| Symbol | Pin(s) | Parameter | Remark/Test Conditions | Min | Typ | Max | Unit |
|--------|--------|-----------|------------------------|-----|-----|-----|------|
|--------|--------|-----------|------------------------|-----|-----|-----|------|

SUPPLY AND VOLTAGE REGULATORS

| | | | | | | | |
|----------------|-----------------------------|--|-------------------------------------|------|---|------|----|
| V_{BB} | V_{BB} | Nominal operating supply range | | 6 | | 30 | V |
| I_{BB} | | Total current consumption (Note 6) | Unloaded outputs | | | 8 | mA |
| V_{DD} | V_{DD} | Regulated output voltage | | 4.50 | 5 | 5.50 | V |
| I_{INT} | | Internal load current (Note 6) | Unloaded outputs | | | 8 | mA |
| I_{LOAD} | | Max output current (external and internal loads) | $6\text{ V} < V_{BB} < 8\text{ V}$ | 20 | | | mA |
| | | | $8\text{ V} < V_{BB} < 30\text{ V}$ | 50 | | | mA |
| I_{DDLIM} | | Current limitation | Pin shorted to ground | | | 150 | mA |
| I_{LOAD_PD} | Output current in powerdown | | 1 | | | mA | |

POWER-ON-RESET (POR)

| | | | | | | | |
|-----------|----------|-----------------------------------|------------------|-----|------|-----|---|
| V_{DDH} | V_{DD} | Internal POR comparator threshold | V_{DD} rising | 4.0 | 4.25 | 4.4 | V |
| V_{DDL} | | Internal POR comparator threshold | V_{DD} falling | | 3.68 | | V |

MOTORDRIVER

| | | | | | | | |
|------------------|--|---|---|-----|------|----------|----------|
| $I_{MDmax,Peak}$ | MOTXP MOTXN MOTYP MOTYN | Max current through motor coil in normal operation | | | 3015 | | mA |
| $I_{MDmax,RMS}$ | | Max RMS current through coil in normal operation | | | 2132 | | mA |
| I_{MDabs} | | Absolute error on coil current | | -10 | | 10 | % |
| I_{MDrel} | | Error on current ratio I_{coilx} / I_{coily} | | -7 | | 7 | % |
| I_{SET_TC1} | | Temperature coefficient of coil current set-level, CUR[4:0] = 0...27 | $-40^{\circ}\text{C} \leq T_J \leq 160^{\circ}\text{C}$ | | -250 | | ppm/k |
| I_{SET_TC2} | | Temperature coefficient of coil current set-level, CUR[4:0] = 28...31 | $-40^{\circ}\text{C} \leq T_J \leq 160^{\circ}\text{C}$ | | -460 | | ppm/k |
| R_{HS} | | On-resistance high-side driver, CUR[4:0] = 0...31 (Note 7) | $V_{BB} = 12\text{ V}, T_J = 27^{\circ}\text{C}$ | | | 0.35 | Ω |
| | | | $V_{BB} = 12\text{ V}, T_J = 160^{\circ}\text{C}$ | | 0.47 | 0.70 | Ω |
| R_{LS3} | | On-resistance low-side driver, CUR[4:0] = 23...31 (Note 7) | $V_{BB} = 12\text{ V}, T_J = 27^{\circ}\text{C}$ | | | 0.35 | Ω |
| | | | $V_{BB} = 12\text{ V}, T_J = 160^{\circ}\text{C}$ | | 0.56 | 0.70 | Ω |
| R_{LS2} | | On-resistance low-side driver, CUR[4:0] = 16...22 (Note 7) | $V_{BB} = 12\text{ V}, T_J = 27^{\circ}\text{C}$ | | | 0.65 | Ω |
| | | | $V_{BB} = 12\text{ V}, T_J = 160^{\circ}\text{C}$ | | 0.9 | 1.25 | Ω |
| R_{LS1} | | On-resistance low-side driver, CUR[4:0] = 9...15 (Note 7) | $V_{BB} = 12\text{ V}, T_J = 27^{\circ}\text{C}$ | | | 1.25 | Ω |
| | $V_{BB} = 12\text{ V}, T_J = 160^{\circ}\text{C}$ | | | 1.7 | 2.5 | Ω | |
| R_{LS0} | On-resistance low-side driver, CUR[4:0] = 0...8 (Note 7) | $V_{BB} = 12\text{ V}, T_J = 27^{\circ}\text{C}$ | | | 2.5 | Ω | |
| | | $V_{BB} = 12\text{ V}, T_J = 160^{\circ}\text{C}$ | | 3.2 | 5.0 | Ω | |
| I_{Mpd} | Pulldown current | HiZ mode | | | 5.0 | mA | |

DIGITAL INPUTS

| | | | | | | | |
|---------------|---|----------------------------|-----------------------------|------|--|----------|------------------|
| I_{leak} | DI, CLK NXT, DIR CLR, \overline{CS} | Input leakage (Note 8) | $T_J = 160^{\circ}\text{C}$ | | | 1 | μA |
| V_{inL} | | Logic low threshold | | 0 | | 0.65 | V |
| V_{inH} | | Logic high threshold | | 2.35 | | V_{DD} | V |
| R_{pd_CLR} | CLR | Internal pulldown resistor | | 120 | | 300 | $\text{k}\Omega$ |
| R_{pd_TST} | TST0 | Internal pulldown resistor | | 3 | | 9 | $\text{k}\Omega$ |

6. Current with oscillator running, all analogue cells active, SPI communication and NXT pulses applied. No floating inputs. Parameter guaranteed by design.
7. Characterization Data Only
8. Not valid for pins with internal pulldown resistor.

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Table 5. DC PARAMETERS (The DC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise specified) Convention: currents flowing in the circuit are defined as positive.

| Symbol | Pin(s) | Parameter | Remark/Test Conditions | Min | Typ | Max | Unit |
|--------|--------|-----------|------------------------|-----|-----|-----|------|
|--------|--------|-----------|------------------------|-----|-----|-----|------|

DIGITAL OUTPUTS

| | | | | | | | |
|----------|-----------------|----------------------------|-------------------------|--|--|-----|---|
| V_{OL} | DO, ERR, POR/WD | Logic Low level open drain | $I_{OL} = 5 \text{ mA}$ | | | 0.5 | V |
|----------|-----------------|----------------------------|-------------------------|--|--|-----|---|

THERMAL WARNING AND SHUTDOWN

| | | | | | | | |
|-----------|--|-----------------------------------|--|-----|---------------|-----|----|
| T_{tw} | | Thermal warning | | 138 | 145 | 152 | °C |
| T_{tsd} | | Thermal shutdown (Notes 9 and 10) | | | $T_{tw} + 20$ | | °C |

CHARGE PUMP

| | | | | | | | |
|--------------|---------|---------------------------|--|--------------|--------------------|---------------|----|
| V_{cp} | VCP | Output voltage | $6 \text{ V} < V_{BB} < 15 \text{ V}$ | | $2 * V_{BB} - 1.5$ | | V |
| | | | $15 \text{ V} < V_{BB} < 30 \text{ V}$ | $V_{BB} + 8$ | $V_{BB} + 11.5$ | $V_{BB} + 15$ | V |
| C_{buffer} | | External buffer capacitor | | 180 | 220 | 470 | nF |
| C_{pump} | CPP CPN | External pump capacitor | | 180 | 220 | 470 | nF |

PACKAGE THERMAL RESISTANCE VALUE

| | | | | | | | |
|------------|------|--|---|--|------|--|-----|
| R_{thja} | NQFP | Thermal Resistance Junction-to-Ambient | Simulated Conform JEDEC JESD-51, (2S2P) | | 30 | | K/W |
| R_{thjp} | | Thermal Resistance Junction-to-Exposed Pad | | | 0.95 | | K/W |

SPEED AND LOAD ANGLE OUTPUT

| | | | | | | | |
|------------|--------------------------|---------------------------------------|----------|-----|------|----------------|----|
| V_{out} | SLA | Output Voltage Range | | 0.2 | | $V_{DD} - 0.2$ | V |
| V_{off} | | Output Offset SLA Pin | SLAG = 0 | -50 | | 50 | mV |
| | | | SLAG = 1 | -30 | | 30 | mV |
| G_{sla} | | Gain of SLA Pin = V_{BEMF}/V_{coil} | SLAG = 0 | | 0.5 | | |
| | | | SLAG = 1 | | 0.25 | | |
| R_{out} | | Output Resistance SLA Pin | | | 0.23 | 1.0 | kΩ |
| C_{LOAD} | Load Capacitance SLA Pin | | | | 50 | pF | |

9. No more than 100 cumulated hours in life time above T_{tw} .

10. Thermal shutdown is derived from thermal warning Characterization Data Only.

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Table 6. AC PARAMETERS (The AC parameters are given for V_{BB} and temperature in their operating ranges)

| Symbol | Pin(s) | Parameter | Remark/Test Conditions | Min | Typ | Max | Unit |
|----------------------------|----------|--|--|------|------|------|-------------|
| INTERNAL OSCILLATOR | | | | | | | |
| f_{osc} | | Frequency of internal oscillator | | 3.6 | 4.0 | 4.4 | MHz |
| MOTORDRIVER | | | | | | | |
| f_{PWM} | MOTxx | PWM frequency | Frequency depends only on internal oscillator | 20.8 | 22.8 | 24.8 | kHz |
| | | Double PWM frequency | | 41.6 | 45.6 | 49.6 | kHz |
| f_d | | PWM Jitter depth (Note 11) | | | 10 | | % f_{PWM} |
| $T_{b_{rise}}$ | MOTxx | Turn-on voltage slope, 10% to 90% | EMC[1:0] = 00 | | 350 | | V/ μ s |
| | | | EMC[1:0] = 01 | | 250 | | V/ μ s |
| | | | EMC[1:0] = 10 | | 200 | | V/ μ s |
| | | | EMC[1:0] = 11 | | 100 | | V/ μ s |
| $T_{b_{fall}}$ | MOTxx | Turn-off voltage slope, 90% to 10% | EMC[1:0] = 00 | | 350 | | V/ μ s |
| | | | EMC[1:0] = 01 | | 250 | | V/ μ s |
| | | | EMC[1:0] = 10 | | 200 | | V/ μ s |
| | | | EMC[1:0] = 11 | | 100 | | V/ μ s |
| DIGITAL OUTPUTS | | | | | | | |
| T_{H2L} | DO ERR | Output fall-time from V_{inH} to V_{inL} | Capacitive load 400 pF and pullup resistor of 1.5 k Ω | | | 50 | ns |
| CHARGE PUMP | | | | | | | |
| f_{CP} | CPN CPP | Charge pump frequency | | | 250 | | kHz |
| T_{CPU} | MOTxx | Start-up time of charge pump (Note 12) | Spec external components in Table 8 | | | 5 | ms |
| CLR FUNCTION | | | | | | | |
| T_{CLR} | CLR | Hard reset duration time | | 100 | | | μ s |
| POWERUP | | | | | | | |
| t_{PU} | POR / WD | Powerup time | $V_{BB} = 12$ V, $I_{LOAD} = 50$ mA, $C_{LOAD} = 220$ nF | | | 110 | μ s |
| t_{POR} | | Reset duration | See Figure 16 | | 100 | | ms |
| t_{RF} | | Reset filter time | See Figure 16 | | 1.0 | | μ s |
| WATCHDOG | | | | | | | |
| t_{WDTO} | POR / WD | Watchdog time out interval | | 32 | | 512 | ms |
| t_{WDPR} | | Prohibited watchdog acknowledge delay | | | 2.0 | | ms |
| NXT FUNCTION | | | | | | | |
| t_{NXT_HI} | NXT | NXT Minimum, High Pulse Width | See Figure 5 | 2.0 | | | μ s |
| t_{NXT_LO} | | NXT Minimum, Low Pulse Width | See Figure 5 | 2.0 | | | μ s |
| t_{DIR_SET} | | NXT Hold Time, Following Change of DIR | See Figure 5 | 0.5 | | | μ s |
| t_{DIR_HOLD} | | NXT Hold Time, Before Change of DIR | See Figure 5 | 0.5 | | | μ s |

11. Characterization Data Only

12. Guaranteed by design

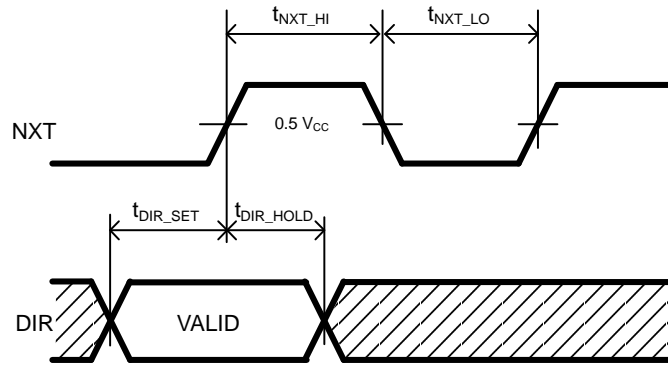


Figure 5. NXT-Input Timing Diagram

Table 7. SPI TIMING PARAMETERS

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------------|--|-----|-----|-----|---------|
| t_{CLK} | SPI Clock Period | 1 | | | μs |
| t_{CLK_HIGH} | SPI Clock High Time | 100 | | | ns |
| t_{CLK_LOW} | SPI Clock Low Time | 100 | | | ns |
| t_{SET_DI} | DI Set Up Time, Valid Data Before Rising Edge of CLK | 50 | | | ns |
| t_{HOLD_DI} | DI Hold Time, Hold Data After Rising Edge of CLK | 50 | | | ns |
| t_{CSB_HIGH} | \overline{CS} High Time | 2.5 | | | μs |
| t_{SET_CSB} | \overline{CS} Set Up Time, \overline{CS} Low Before Rising Edge of CLK | 100 | | | ns |
| t_{SET_CLK} | CLK Set Up Time, CLK Low Before Rising Edge of \overline{CS} | 100 | | | ns |

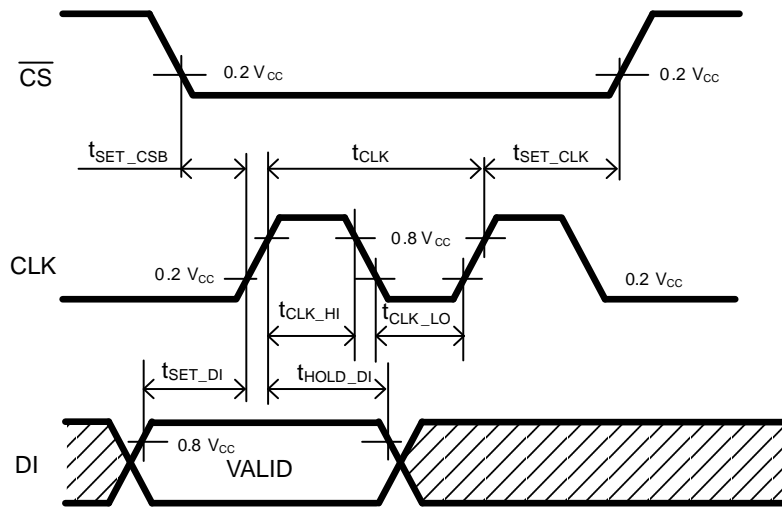


Figure 6. SPI Timing

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TYPICAL APPLICATION SCHEMATIC

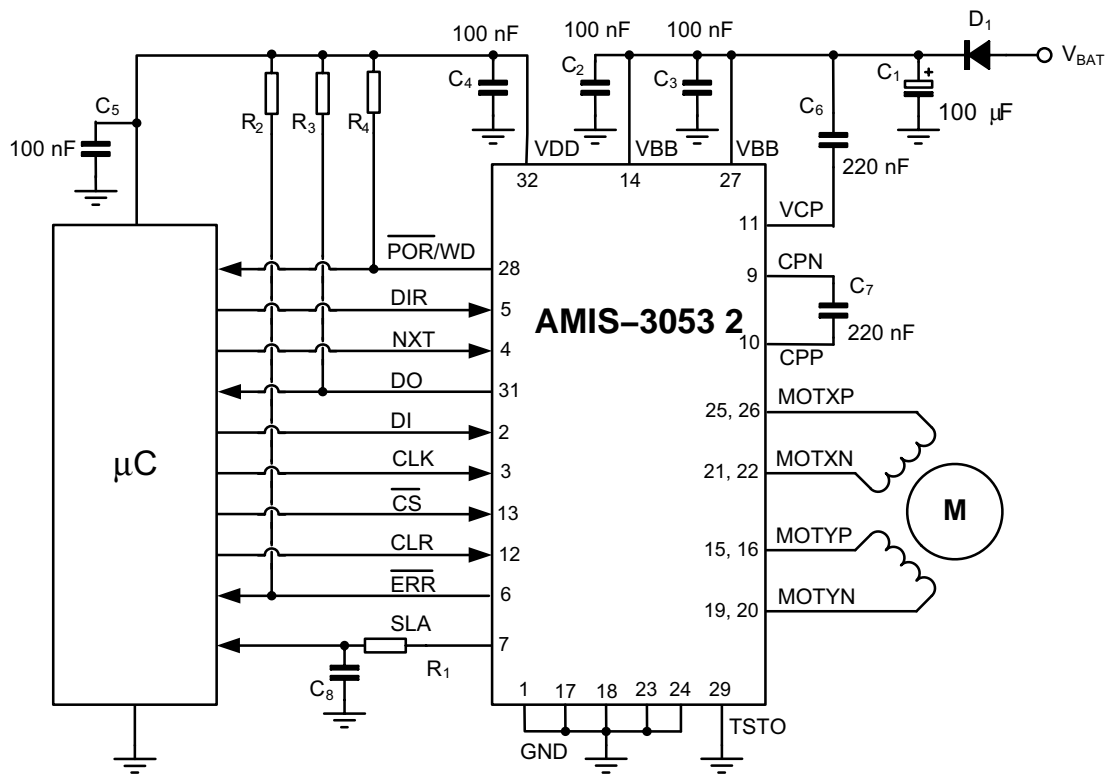


Figure 7. Typical Application Schematic AMIS-30532

Table 8. EXTERNAL COMPONENTS LIST AND DESCRIPTION

| Component | Function | Typ Value | Tolerance | Unit |
|--|--|-----------|-----------|------|
| C ₁ | V _{BB} Buffer Capacitor (Note 13) | 100 | -20 +80% | μF |
| C ₂ , C ₃ | V _{BB} Decoupling Block Capacitor | 100 | -20 +80% | nF |
| C ₄ | V _{DD} Buffer Capacitor | 100 | ± 20% | nF |
| C ₅ | V _{DD} Buffer Capacitor | 100 | ± 20% | nF |
| C ₆ | Charge Pump Buffer Capacitor | 220 | ± 20% | nF |
| C ₇ | Charge Pump Pumping Capacitor | 220 | ± 20% | nF |
| C ₈ | Low Pass Filter SLA | 1 | ± 20% | nF |
| R ₁ | Low Pass Filter SLA | 5.6 | ± 1% | kΩ |
| R ₂ , R ₃ , R ₄ | Pullup Resistor Open Drain Output | 4.7 | ± 1% | kΩ |
| D ₁ | Optional Reverse Protection Diode | MURD530 | | |

13. ESR < 1 Ω.

FUNCTIONAL DESCRIPTION

H-Bridge Drivers

A full H-bridge is integrated for each of the two stator windings. Each H-bridge consists of two low-side and two high-side N-type MOSFET switches. Writing logic ‘0’ in bit <MOTEN> disables all drivers (high-impedance). Writing logic ‘1’ in this bit enables both bridges and current can flow in the motor stator windings.

In order to avoid large currents through the H-bridge switches, it is guaranteed that the top- and bottom-switches of the same half-bridge are never conductive simultaneously (interlock delay).

A two-stage protection against shorts on motor lines is implemented. In a first stage, the current in the driver is limited. Secondly, when excessive voltage is sensed across the transistor, the transistor is switched-off.

In order to reduce the radiated/conducted emission, voltage slope control is implemented in the output switches. The output slope is defined by the gate-drain capacitance of output transistor and the (limited) current that drives the gate. There are two trimming bits for slope control (see SPI Control Parameter Overview EMC[1:0]).

The power transistors are equipped with so-called “active diodes”: when a current is forced trough the transistor switch in the reverse direction, i.e. from source to drain, then the transistor is switched on. This ensures that most of the current flows through the channel of the transistor instead of through the inherent parasitic drain-bulk diode of the transistor.

Depending on the desired current range and the micro-step position at hand, the $R_{DS(on)}$ of the low-side

transistors will be adapted such that excellent current-sense accuracy is maintained. The $R_{DS(on)}$ of the high-side transistors remain unchanged, see Table 5 DC Parameters for more details.

PWM Current Control

A PWM comparator compares continuously the actual winding current with the requested current and feeds back the information to a digital regulation loop. This loop then generates a PWM signal, which turns on/off the H-bridge switches. The switching points of the PWM duty-cycle are synchronized to the on-chip PWM clock. The frequency of the PWM controller can be doubled and an artificial jitter can be added (see SPI Control Parameter Overview PWMJ). The PWM frequency will not vary with changes in the supply voltage. Also variations in motor-speed or load-conditions of the motor have no effect. There are no external components required to adjust the PWM frequency.

Automatic Forward and Slow-Fast Decay

The PWM generation is in steady-state using a combination of forward and slow-decay. The absence of fast-decay in this mode, guarantees the lowest possible current-ripple “by design”. For transients to lower current levels, fast-decay is automatically activated to allow high-speed response. The selection of fast or slow decay is completely transparent for the user and no additional parameters are required for operation.

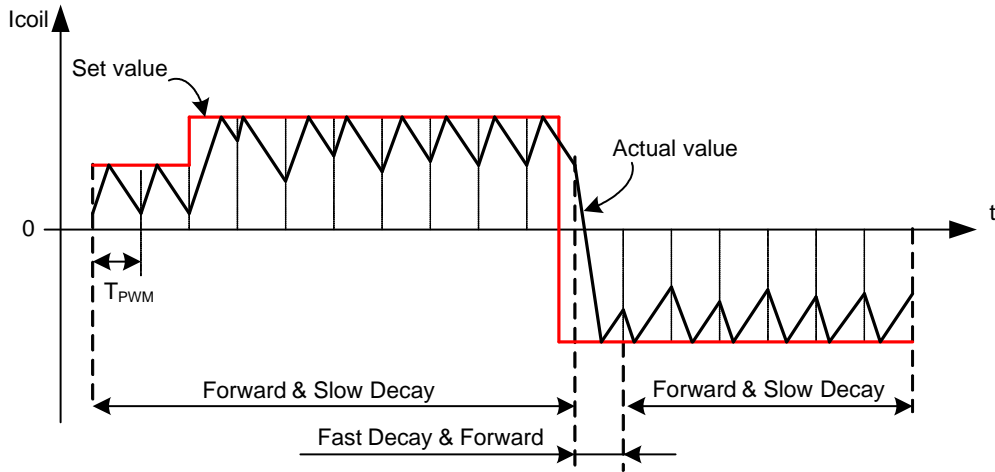


Figure 8. Forward and Slow/Fast Decay PWM

Automatic Duty Cycle Adaptation

In case the supply voltage is lower than $2 \cdot B_{emf}$, then the duty cycle of the PWM is adapted automatically to $> 50\%$ to maintain the requested average current in the coils. This

process is completely automatic and requires no additional parameters for operation. The over-all current-ripple is divided by two if PWM frequency is doubled (see SPI Control Parameter Overview PWMF).

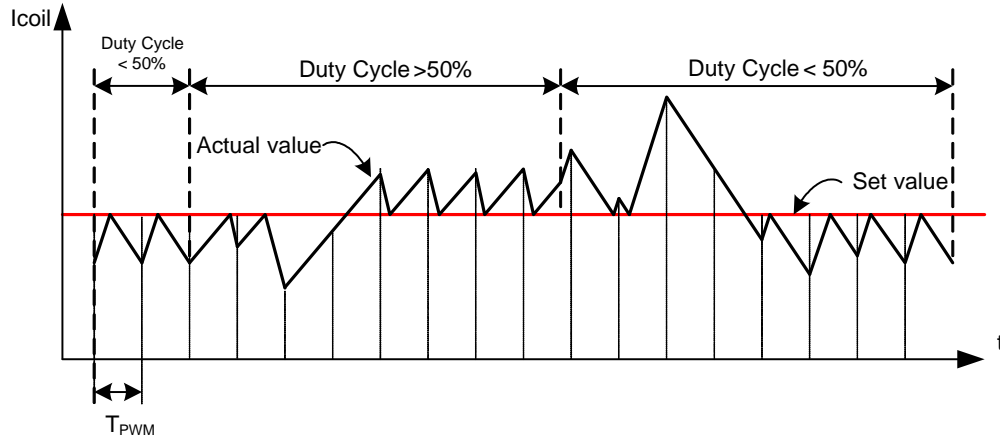


Figure 9. Automatic Duty Cycle Adaptation

Step Translator and Step Mode

The step translator provides the control of the motor by means of SPI register Stepmode: SM[2:0], SPI register DIRCNTRL, and input pins DIR and NXT. It is translating consecutive steps in corresponding currents in both motor coils for a given step mode.

One out of seven possible stepping modes can be selected through SPI-bits SM[2:0] (see SPI Control Parameter Overview). After power-on or hard reset, the coil-current translator is set to the default 1/32 micro-stepping at position '0'. Upon changing the step mode, the translator jumps to position 0* of the corresponding stepping mode.

When remaining in the same step mode, subsequent translator positions are all in the same column and increased or decreased with 1. Table 10 lists the output current versus the translator position.

As shown in Figure 10 the output current-pairs can be projected approximately on a circle in the (I_x, I_y) plane. There are, however, two exceptions: uncompensated half step and full step. In these step modes the currents are not regulated to a fraction of I_{max} but are in all intermediate steps regulated at 100%. In the (I_x, I_y) plane the current-pairs are projected on a square. Table 9 lists the output current versus the translator position for these cases.

Table 9. SQUARE TRANSLATOR TABLE FOR FULL STEP AND UNCOMPENSATED HALF STEP

| MSP[6:0] | Stepmode (SM[2:0]) | | % of I_{max} | |
|----------|-------------------------|-----------|----------------|--------|
| | 101 | 110 | Coil x | Coil y |
| | Uncompensated Half-Step | Full Step | | |
| 000 0000 | 0* | - | 0 | 100 |
| 001 0000 | 1 | 1 | 100 | 100 |
| 010 0000 | 2 | - | 100 | 0 |
| 011 0000 | 3 | 2 | 100 | -100 |
| 100 0000 | 4 | - | 0 | -100 |
| 101 0000 | 5 | 3 | -100 | -100 |
| 110 0000 | 6 | - | -100 | 0 |
| 111 0000 | 7 | 0 | -100 | 100 |

Table 10. CIRCULAR TRANSLATOR TABLE

| MSP[6:0] | Stepmode (SM[2:0]) | | | | | % of I _{max} | |
|----------|--------------------|------|-----|-----|-----|-----------------------|--------|
| | 000 | 001 | 010 | 011 | 100 | Coil x | Coil y |
| | 1/32 | 1/16 | 1/8 | 1/4 | 1/2 | | |
| 000 0000 | 0' | 0* | 0* | 0* | 0* | 0 | 100 |
| 000 0001 | 1 | - | - | - | - | 3.5 | 98.8 |
| 000 0010 | 2 | 1 | - | - | - | 8.1 | 97.7 |
| 000 0011 | 3 | - | - | - | - | 12.7 | 96.5 |
| 000 0100 | 4 | 2 | 1 | - | - | 17.4 | 95.3 |
| 000 0101 | 5 | - | - | - | - | 22.1 | 94.1 |
| 000 0110 | 6 | 3 | - | - | - | 26.7 | 93 |
| 000 0111 | 7 | - | - | - | - | 31.4 | 91.8 |
| 000 1000 | 8 | 4 | 2 | 1 | - | 34.9 | 89.5 |
| 000 1001 | 9 | - | - | - | - | 38.3 | 87.2 |
| 000 1010 | 10 | 5 | - | - | - | 43 | 84.9 |
| 000 1011 | 11 | - | - | - | - | 46.5 | 82.6 |
| 000 1100 | 12 | 6 | 3 | - | - | 50 | 79 |
| 000 1101 | 13 | - | - | - | - | 54.6 | 75.5 |
| 000 1110 | 14 | 7 | - | - | - | 58.1 | 72.1 |
| 000 1111 | 15 | - | - | - | - | 61.6 | 68.6 |
| 001 0000 | 16 | 8 | 4 | 2 | 1 | 65.1 | 65.1 |
| 001 0001 | 17 | - | - | - | - | 68.6 | 61.6 |
| 001 0010 | 18 | 9 | - | - | - | 72.1 | 58.1 |
| 001 0011 | 19 | - | - | - | - | 75.5 | 54.6 |
| 001 0100 | 20 | 10 | 5 | - | - | 79 | 50 |
| 001 0101 | 21 | - | - | - | - | 82.6 | 46.5 |
| 001 0110 | 22 | 11 | - | - | - | 84.9 | 43 |
| 001 0111 | 23 | - | - | - | - | 87.2 | 38.3 |
| 001 1000 | 24 | 12 | 6 | 3 | - | 89.5 | 34.9 |
| 001 1001 | 25 | - | - | - | - | 91.8 | 31.4 |
| 001 1010 | 26 | 13 | - | - | - | 93 | 26.7 |
| 001 1011 | 27 | - | - | - | - | 94.1 | 22.1 |
| 001 1100 | 28 | 14 | 7 | - | - | 95.3 | 17.4 |
| 001 1101 | 29 | - | - | - | - | 96.5 | 12.7 |
| 001 1110 | 30 | 15 | - | - | - | 97.7 | 8.1 |
| 001 1111 | 31 | - | - | - | - | 98.8 | 3.5 |
| 010 0000 | 32 | 16 | 8 | 4 | 2 | 100 | 0 |
| 010 0001 | 33 | - | - | - | - | 98.8 | -3.5 |
| 010 0010 | 34 | 17 | - | - | - | 97.7 | -8.1 |
| 010 0011 | 35 | - | - | - | - | 96.5 | -12.7 |
| 010 0100 | 36 | 18 | 9 | - | - | 95.3 | -17.4 |
| 010 0101 | 37 | - | - | - | - | 94.1 | -22.1 |
| 010 0110 | 38 | 19 | - | - | - | 93 | -26.7 |
| 010 0111 | 39 | - | - | - | - | 91.8 | -31.4 |
| 010 1000 | 40 | 20 | 10 | 5 | - | 89.5 | -34.9 |
| 010 1001 | 41 | - | - | - | - | 87.2 | -38.3 |
| 010 1010 | 42 | 21 | - | - | - | 84.9 | -43 |
| 010 1011 | 43 | - | - | - | - | 82.6 | -46.5 |
| 010 1100 | 44 | 22 | 11 | - | - | 79 | -50 |
| 010 1101 | 45 | - | - | - | - | 75.5 | -54.6 |
| 010 1110 | 46 | 23 | - | - | - | 72.1 | -58.1 |
| 010 1111 | 47 | - | - | - | - | 68.6 | -61.6 |
| 011 0000 | 48 | 24 | 12 | 6 | 3 | 65.1 | -65.1 |
| 011 0001 | 49 | - | - | - | - | 61.6 | -68.6 |
| 011 0010 | 50 | 25 | - | - | - | 58.1 | -72.1 |
| 011 0011 | 51 | - | - | - | - | 54.6 | -75.5 |
| 011 0100 | 52 | 26 | 13 | - | - | 50 | -79 |
| 011 0101 | 53 | - | - | - | - | 46.5 | -82.6 |
| 011 0110 | 54 | 27 | - | - | - | 43 | -84.9 |
| 011 0111 | 55 | - | - | - | - | 38.3 | -87.2 |
| 011 1000 | 56 | 28 | 14 | 7 | - | 34.9 | -89.5 |
| 011 1001 | 57 | - | - | - | - | 31.4 | -91.8 |
| 011 1010 | 58 | 29 | - | - | - | 26.7 | -93 |
| 011 1011 | 59 | - | - | - | - | 22.1 | -94.1 |
| 011 1100 | 60 | 30 | 15 | - | - | 17.4 | -95.3 |
| 011 1101 | 61 | - | - | - | - | 12.7 | -96.5 |
| 011 1110 | 62 | 31 | - | - | - | 8.1 | -97.7 |
| 011 1111 | 63 | - | - | - | - | 3.5 | -98.8 |

Table 11. CIRCULAR TRANSLATOR TABLE (CONTINUED)

| MSP[6:0] | Stepmode (SM[2:0]) | | | | | % of I _{max} | |
|----------|--------------------|------|-----|-----|-----|-----------------------|--------|
| | 000 | 001 | 010 | 011 | 100 | Coil x | Coil y |
| | 1/32 | 1/16 | 1/8 | 1/4 | 1/2 | | |
| 100 0000 | 64 | 32 | 16 | 8 | 4 | 0 | -100 |
| 100 0001 | 65 | - | - | - | - | -3.5 | -98.8 |
| 100 0010 | 66 | 33 | - | - | - | -8.1 | -97.7 |
| 100 0011 | 67 | - | - | - | - | -12.7 | -96.5 |
| 100 0100 | 68 | 34 | 17 | - | - | -17.4 | -95.3 |
| 100 0101 | 69 | - | - | - | - | -22.1 | -94.1 |
| 100 0110 | 70 | 35 | - | - | - | -26.7 | -93 |
| 100 0111 | 71 | - | - | - | - | -31.4 | -91.8 |
| 100 1000 | 72 | 36 | 18 | 9 | - | -34.9 | -89.5 |
| 100 1001 | 73 | - | - | - | - | -38.3 | -87.2 |
| 100 1010 | 74 | 37 | - | - | - | -43 | -84.9 |
| 100 1011 | 75 | - | - | - | - | -46.5 | -82.6 |
| 100 1100 | 76 | 38 | 19 | - | - | -50 | -79 |
| 100 1101 | 77 | - | - | - | - | -54.6 | -75.5 |
| 100 1110 | 78 | 39 | - | - | - | -58.1 | -72.1 |
| 100 1111 | 79 | - | - | - | - | -61.6 | -68.6 |
| 101 0000 | 80 | 40 | 20 | 10 | 5 | -65.1 | -65.1 |
| 101 0001 | 81 | - | - | - | - | -68.6 | -61.6 |
| 101 0010 | 82 | 41 | - | - | - | -72.1 | -58.1 |
| 101 0011 | 83 | - | - | - | - | -75.5 | -54.6 |
| 101 0100 | 84 | 42 | 21 | - | - | -79 | -50 |
| 101 0101 | 85 | - | - | - | - | -82.6 | -46.5 |
| 101 0110 | 86 | 43 | - | - | - | -84.9 | -43 |
| 101 0111 | 87 | - | - | - | - | -87.2 | -38.3 |
| 101 1000 | 88 | 44 | 22 | 11 | - | -89.5 | -34.9 |
| 101 1001 | 89 | - | - | - | - | -91.8 | -31.4 |
| 101 1010 | 90 | 45 | - | - | - | -93 | -26.7 |
| 101 1011 | 91 | - | - | - | - | -94.1 | -22.1 |
| 101 1100 | 92 | 46 | 23 | - | - | -95.3 | -17.4 |
| 101 1101 | 93 | - | - | - | - | -96.5 | -12.7 |
| 101 1110 | 94 | 47 | - | - | - | -97.7 | -8.1 |
| 101 1111 | 95 | - | - | - | - | -98.8 | -3.5 |
| 110 0000 | 96 | 48 | 24 | 12 | 6 | -100 | 0 |
| 110 0001 | 97 | - | - | - | - | -98.8 | 3.5 |
| 110 0010 | 98 | 49 | - | - | - | -97.7 | 8.1 |
| 110 0011 | 99 | - | - | - | - | -96.5 | 12.7 |
| 110 0100 | 100 | 50 | 25 | - | - | -95.3 | 17.4 |
| 110 0101 | 101 | - | - | - | - | -94.1 | 22.1 |
| 110 0110 | 102 | 51 | - | - | - | -93 | 26.7 |
| 110 0111 | 103 | - | - | - | - | -91.8 | 31.4 |
| 110 1000 | 104 | 52 | 26 | 13 | - | -89.5 | 34.9 |
| 110 1001 | 105 | - | - | - | - | -87.2 | 38.3 |
| 110 1010 | 106 | 53 | - | - | - | -84.9 | 43 |
| 110 1011 | 107 | - | - | - | - | -82.6 | 46.5 |
| 110 1100 | 108 | 54 | 27 | - | - | -79 | 50 |
| 110 1101 | 109 | - | - | - | - | -75.5 | 54.6 |
| 110 1110 | 110 | 55 | - | - | - | -72.1 | 58.1 |
| 110 1111 | 111 | - | - | - | - | -68.6 | 61.6 |
| 111 0000 | 112 | 56 | 28 | 14 | 7 | -65.1 | 65.1 |
| 111 0001 | 113 | - | - | - | - | -61.6 | 68.6 |
| 111 0010 | 114 | 57 | - | - | - | -58.1 | 72.1 |
| 111 0011 | 115 | - | - | - | - | -54.6 | 75.5 |
| 111 0100 | 116 | 58 | 29 | - | - | -50 | 79 |
| 111 0101 | 117 | - | - | - | - | -46.5 | 82.6 |
| 111 0110 | 118 | 59 | - | - | - | -43 | 84.9 |
| 111 0111 | 119 | - | - | - | - | -38.3 | 87.2 |
| 111 1000 | 120 | 60 | 30 | 15 | - | -34.9 | 89.5 |
| 111 1001 | 121 | - | - | - | - | -31.4 | 91.8 |
| 111 1010 | 122 | 61 | - | - | - | -26.7 | 93 |
| 111 1011 | 123 | - | - | - | - | -22.1 | 94.1 |
| 111 1100 | 124 | 62 | 31 | - | - | -17.4 | 95.3 |
| 111 1101 | 125 | - | - | - | - | -12.7 | 96.5 |
| 111 1110 | 126 | 63 | - | - | - | -8.1 | 97.7 |
| 111 1111 | 127 | - | - | - | - | -3.5 | 98.8 |

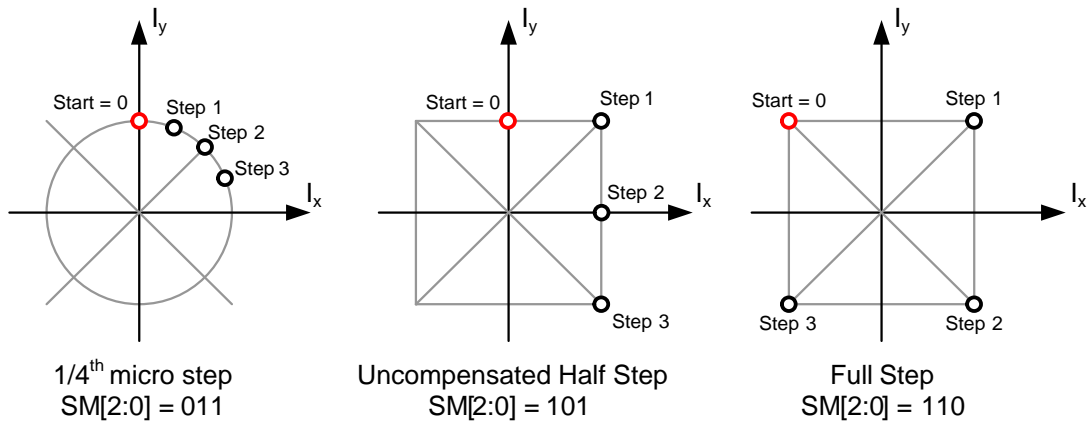


Figure 10. Translator Table: Circular and Square

Direction

The direction of rotation is selected by means of following combination of the DIR input pin and the SPI-controlled direction bit <DIRCTRL>. (see Table 14 SPI Control Parameter Overview)

NXT Input

Changes on the NXT input will move the motor current one step up/down in the translator table (even when the motor is disabled <MOTEN>=0>). Depending on the

NXT-polarity bit <NXTP> (see Table 14 SPI Control Parameter Overview), the next step is initiated either on the rising edge or the falling edge of the NXT input.

Translator Position

The translator position MSP[6:0] can be read in SPI Status Register 3 (See Table 15 SR3). This is a 7-bit number equivalent to the 1/32th micro-step from Table 10: Circular Translator Table. The translator position is updated immediately following a NXT trigger.

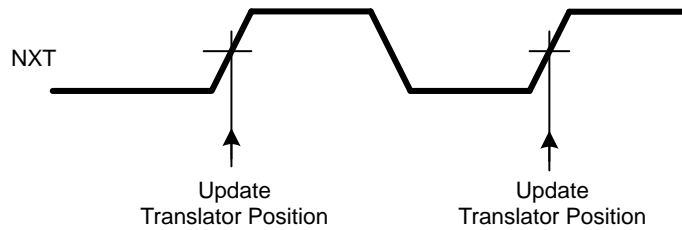


Figure 11. Translator Position Timing Diagram

Synchronization of Step Mode and NXT Input

When step mode is re-programmed to another resolution (Figure 12), then this is put in effect immediately upon the first arriving “NXT” input. If the micro-stepping resolution is increased, the coil currents will be regulated to the nearest micro-step, according to the fixed grid of the increased resolution. If however the micro-stepping resolution is decreased, then it is possible to introduce an offset (or phase shift) in the micro-step translator table.

If the step resolution is decreased at a translator table position that is shared both by the old and new resolution setting, then the offset is zero and micro-stepping is proceeds according to the translator table.

If the translator position is **not** shared both by the old and new resolution setting, then the micro-stepping proceeds with an offset relative to the translator table (See Figure 12 right hand side).

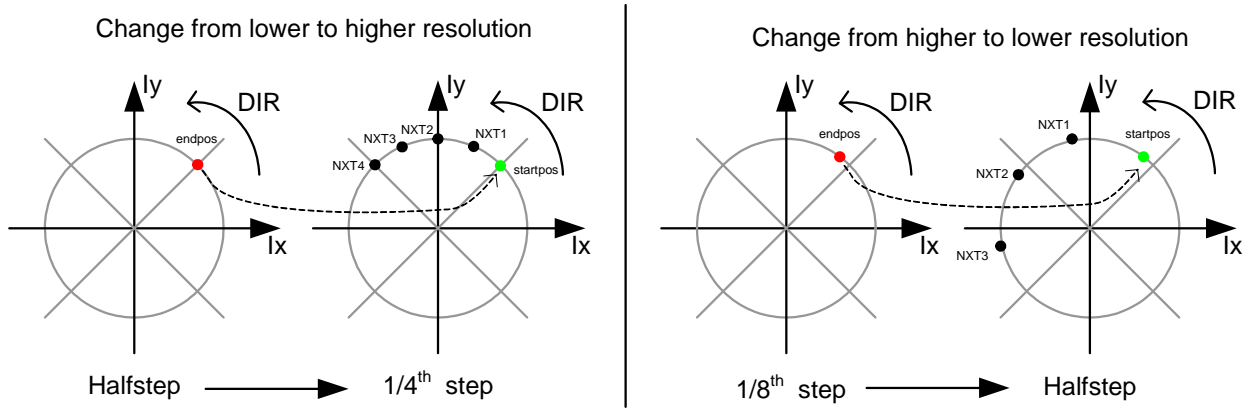


Figure 12. NXT-Step Mode Synchronization

Left: Change from lower to higher resolution. The left-hand side depicts the ending half-step position during which a new step mode resolution was programmed. The right-hand side diagram shows the effect of subsequent NXT commands on the micro-step position.

Right: Change from higher to lower resolution. The left-hand side depicts the ending micro-step position during which a new step mode resolution was programmed. The right-hand side diagram shows the effect of subsequent NXT commands on the half-step position.

Note: It is advised to reduce the micro-stepping resolution only at micro-step positions that overlap with desired micro-step positions of the new resolution.

Programmable Peak-Current

The amplitude of the current waveform in the motor coils (coil peak current = I_{max}) is adjusted by means of an SPI parameter "CUR[4:0]" (see Table 14 SPI Control Parameter

Overview). Whenever this parameter is changed, the coil-currents will be updated immediately at the next PWM period. Figure 13 presents the Peak-Current and Current Ratings in conjunction to the Current setting CUR[4:0].

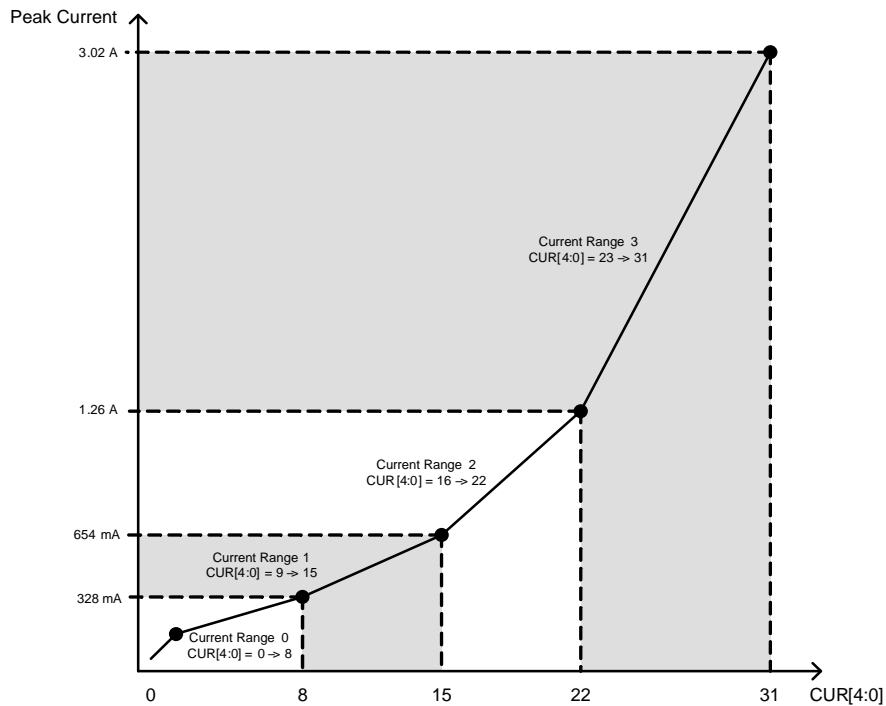


Figure 13. Programmable Peak-Current Overview

Speed and Load Angle Output

The SLA-pin provides an output voltage that indicates the level of the Back-e.m.f. voltage of the motor. This Back-e.m.f. voltage is sampled during every so-called “coil

current zero crossings”. Per coil, two zero-current positions exist per electrical period, yielding in total four zero-current observation points per electrical period.

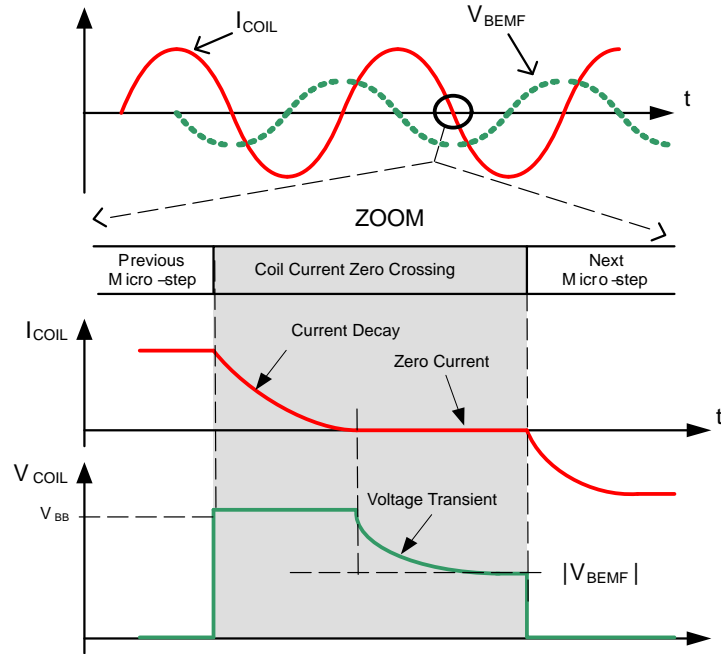


Figure 14. Principle of BEMF Measurement

Because of the relatively high recirculation currents in the coil during current decay, the coil voltage V_{COIL} shows a transient behavior. As this transient is not always desired in application software, two operating modes can be selected by means of the bit <SLAT> (see “SLA-transparency” in see SPI Control Parameter Overview). The SLA pin shows in “transparent mode” full visibility of the voltage transient behavior. This allows a sanity-check of the speed-setting versus motor operation and characteristics and supply voltage levels. If the bit “SLAT” is cleared, then only the voltage samples at the end of each coil current zero crossing are visible on the SLA-pin. Because the transient behavior

of the coil voltage is not visible anymore, this mode generates smoother Back e.m.f. input for post-processing, e.g. by software.

In order to bring the sampled Back e.m.f. to a descent output level (0 V to 5 V), the sampled coil voltage V_{COIL} is divided by 2 or by 4. This divider is set through an SPI bit <SLAG>. (see SPI Control Parameter Overview)

The following drawing illustrates the operation of the SLA-pin and the transparency-bit. “PWMsh” and “ $I_{COIL} = 0$ ” are internal signals that define together with SLAT the sampling and hold moments of the coil voltage.

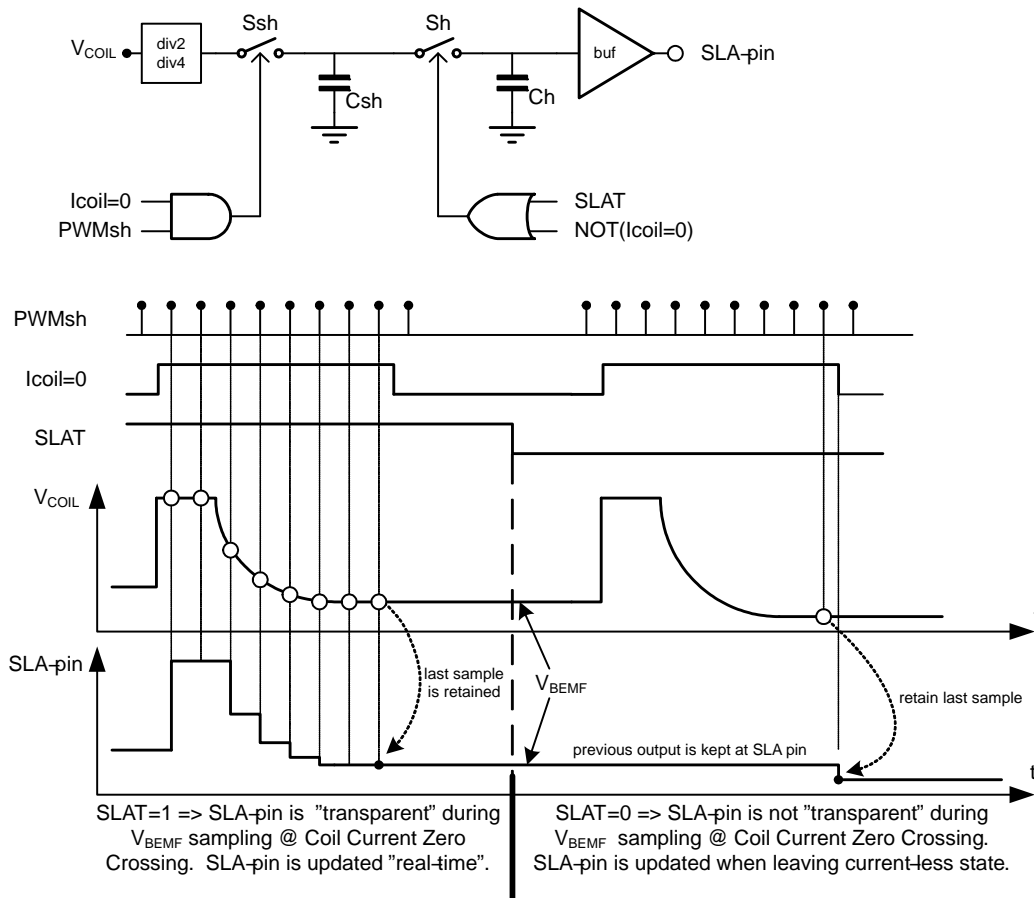


Figure 15. Timing Diagram of SLA-pin

Warning, Error Detection and Diagnostics Feedback

Thermal Warning and Shutdown

When junction temperature rises above T_{TW} , the thermal warning bit <TW> is set (Table 16 SPI Status registers Address SR0). If junction temperature increases above thermal shutdown level, then the circuit goes in "Thermal Shutdown" mode (<TSD>) and all driver transistors are disabled (high impedance) (see Table 16 SPI Status registers Address SR2). The conditions to reset flag <TSD> is to be at a temperature lower than T_{TW} and to clear the <TSD> flag by reading it using any SPI read command.

Overcurrent Detection

The overcurrent detection circuit monitors the load current in each activated output stage. If the load current exceeds the overcurrent detection threshold, then the over-current flag is set and the drivers are switched off to reduce the power dissipation and to protect the integrated circuit. Each driver transistor has an individual detection bit in (see Table 16 SPI Status registers Address SR1 and SR2: <OVXij> and <OVYij>). Error condition is latched and the microcontroller needs to clean the status bits to reactivate the drivers.

Note: Successive reading the SPI StatusRegisters 1 and 2 in case of a short circuit condition, may lead to damage to the drivers.

Open Coil/Current Not Reached Detection

Open coil detection is based on the observation of 100% duty cycle of the PWM regulator. If in a coil 100% duty cycle is detected for longer than 200 ms then the related driver transistors are disabled (high-impedance) and an appropriate bit in the SPI status register is set (<OPENX> or <OPENY>). (Table 16)

When the resistance of a motor coil is very large and the supply voltage is low, it can happen that the motor driver is not able to deliver the requested current to the motor. Under these conditions the PWM controller duty cycle will be 100% and after 200 ms the error pin and <OPENX>, <OPENY> will flag this situation (motor current is kept alive). This feature can be used to test if the operating conditions (supply voltage, motor coil resistance) still allow reaching the requested coil-current or else the coil current should be reduced.

Charge Pump Failure

The charge pump is an important circuit that guarantees low $R_{DS(on)}$ for all drivers, especially for low supply

voltages. If supply voltage is too low or external components are not properly connected to guarantee $R_{DS(on)}$ of the drivers, then the bit <CPFAIL> is set (Table 16). Also after POR the charge pump voltage will need some time to exceed the required threshold. During that time <CPFAIL> will be set to “1”.

Error Output

This is a digital output to flag a problem to the external microcontroller. The signal on this output is active low and the logic combination of:

$$\text{NOT(ERRB)} = \text{<TW> OR <TSD> OR <OVCIj> OR <OVCIj> OR <OPENi> OR <CPFAIL>}$$

Logic Supply Regulator

AMIS-30532 has an on-chip 5 V low-drop regulator with external capacitor to supply the digital part of the chip,

some low-voltage analog blocks and external circuitry. The voltage is derived from an internal bandgap reference. To calculate the available drive-current for external circuitry, the specified I_{load} should be reduced with the consumption of internal circuitry (unloaded outputs) and the loads connected to logic outputs. See Table 5 DC Parameters.

Power-On Reset (POR) Function

The open drain output pin $\overline{\text{POR/WD}}$ provides an “active low” reset for external purposes. At power-up of AMIS-30532, this pin will be kept low for some time to reset for example an external microcontroller. A small analog filter avoids resetting due to spikes or noise on the V_{DD} supply.

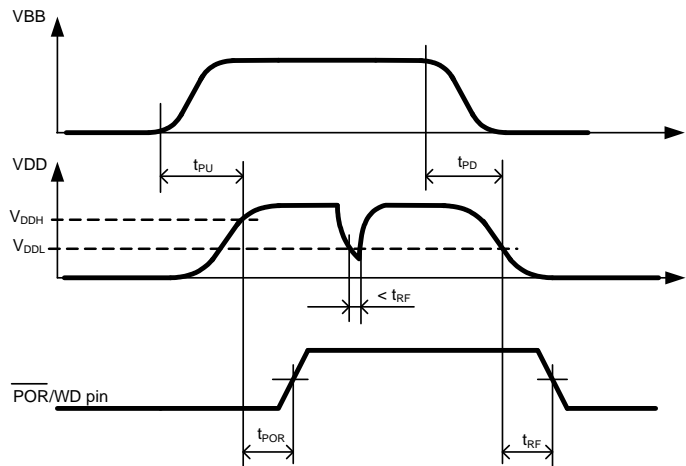


Figure 16. Power-on-Reset Timing Diagram

Watchdog Function

The watchdog function is enabled/disabled through <WDEN> bit (Table 13: SPI CONTROL REGISTERS (ALL SPI control registers have Read/Write Access and default to “0” after power-on or hard reset.)). Once this bit has been set to “1” (watchdog enable), the microcontroller needs to re-write this bit to clear an internal timer before the watchdog timeout interval expires. In case the timer is activated and WDEN is acknowledged too early (before t_{WDPR}) or not within the interval (after t_{WDTO}), then a reset of the microcontroller will occur through $\overline{\text{POR/WD}}$ pin. In addition, a warm/cold boot bit <WD> is available (see Tables 16 and 17) for further processing when the external microcontroller is alive again.

CLR Pin (=Hard Reset)

Logic 0 on CLR pin allows normal operation of the chip. To reset the complete digital inside AMIS-30532, the input CLR needs to be pulled to logic 1 during minimum time given by t_{CLR} . (Table 6 AC Parameters). This reset function clears all internal registers without the need of a power-cycle, except in sleep mode. The operation of all

analog circuits is depending on the reset state of the digital, charge pump remains active. Logic 0 on CLR pin resumes normal operation again.

The voltage regulator remains functional during and after the reset and the $\overline{\text{POR/WD}}$ pin is not activated. Watchdog function is reset completely.

Sleep Mode

The bit <SLP> in SPI Control Register 2 (See Table 12) is provided to enter a so-called “sleep mode”. This mode allows reduction of current-consumption when the motor is not in operation. The effect of sleep mode is as follows:

- The drivers are put in HiZ
- All analog circuits are disabled and in low-power mode
- All internal registers are maintaining their logic content
- NXT and DIR inputs are forbidden
- SPI communication remains possible (slight current increase during SPI communication)
- Reset of chip is possible through CLR pin

- Oscillator and digital clocks are silent, except during SPI communication

The voltage regulator remains active but with reduced current-output capability ($I_{LOADSLP}$). The watchdog timer stops running and its value is kept in the counter. Upon

leaving sleep mode, this timer continues from the value it had before entering sleep mode.

Normal operation is resumed after writing logic '0' to bit <SLP>. A start-up time is needed for the charge pump to stabilize. After this time, NXT commands can be issued.

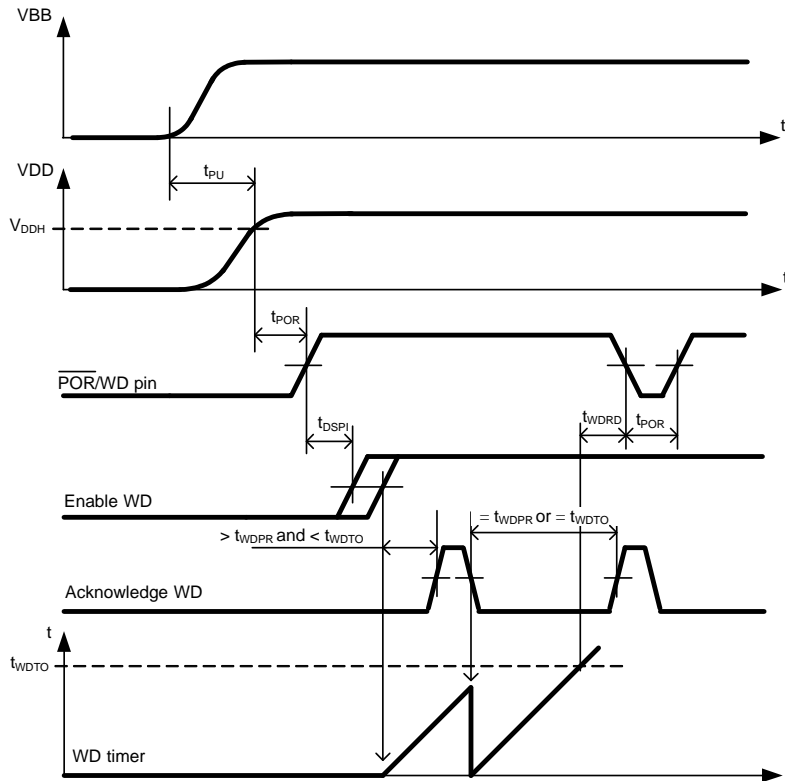


Figure 17. Watchdog Timing Diagram

Note: t_{Dspi} is the time needed by the external microcontroller to shift-in the <WDEN> bit after a power-up.

The duration of the watchdog timeout interval is programmable through the WDT[3:0] bits (See also Table 13: SPI CONTROL REGISTERS (ALL SPI control registers have Read/Write Access and default to “0” after power-on or hard reset.). The timing is given in Table 12 below.

Table 12. WATCHDOG TIMEOUT INTERVAL AS FUNCTION OF WDT[3:0]

| Index WDT[3:0] | | t_{WDT0} (ms) | Index WDT[3:0] | | t_{WDT0} (ms) |
|----------------|------|-----------------|----------------|------|-----------------|
| 0 | 0000 | 32 | 8 | 1000 | 288 |
| 1 | 0001 | 64 | 9 | 1001 | 320 |
| 2 | 0010 | 96 | 10 | 1010 | 352 |
| 3 | 0011 | 128 | 11 | 1011 | 384 |
| 4 | 0100 | 160 | 12 | 1100 | 416 |
| 5 | 0101 | 192 | 13 | 1101 | 448 |
| 6 | 0110 | 224 | 14 | 1110 | 480 |
| 7 | 0111 | 256 | 15 | 1111 | 512 |

SPI INTERFACE

The serial peripheral interface (SPI) allows an external microcontroller (Master) to communicate with AMIS-30532. The implemented SPI block is designed to interface directly with numerous micro-controllers from several manufacturers. AMIS-30532 acts always as a Slave and can't initiate any transmission. The operation of the device is configured and controlled by means of SPI registers which are observable for read and/or write from the Master.

SPI Transfer Format and Pin Signals

During a SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (CLK) synchronizes shifting and sampling of the information on the two serial data lines (DO and DI).

DO signal is the output from the Slave (AMIS-30532), and DI signal is the output from the Master. A chip select line (\overline{CS}) allows individual selection of a Slave SPI device in a multiple-slave system. The \overline{CS} line is active low. If AMIS-30532 is not selected, DO is pulled up with the external pull up resistor. Since AMIS-30532 operates as a Slave in MODE 0 (CPOL = 0; CPHA = 0) it always clocks data out on the falling edge and samples data in on rising edge of clock. The Master SPI port must be configured in MODE 0 too, to match this operation. The SPI clock idles low between the transferred bytes.

The diagram below is both a Master and a Slave timing diagram since CLK, DO and DI pins are directly connected between the Master and the Slave.

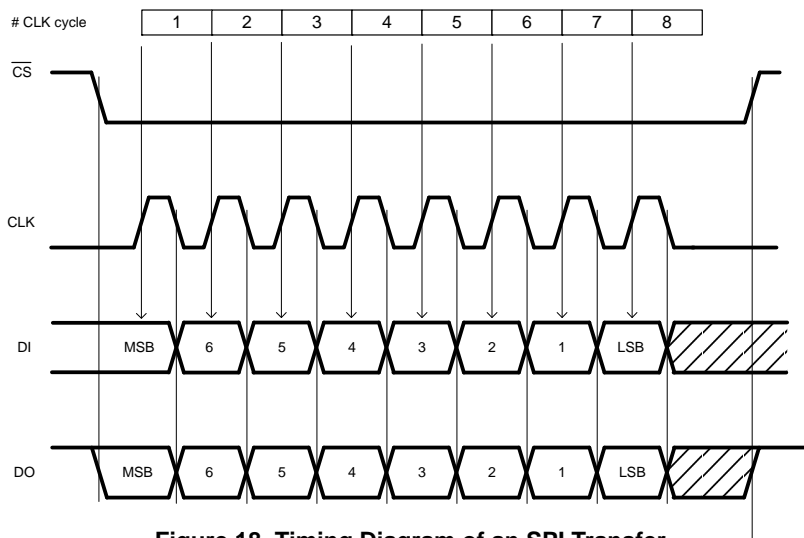


Figure 18. Timing Diagram of an SPI Transfer

NOTE: At the falling edge of the eight clock pulse the data-out shift register is updated with the content of the addressed internal SPI register. The internal SPI registers are updated at the first rising edge of the AMIS-30532 system clock when \overline{CS} = High

Transfer Packet

Serial data transfer is assumed to follow MSB first rule. The transfer packet contains one or more 8-bit characters (bytes).

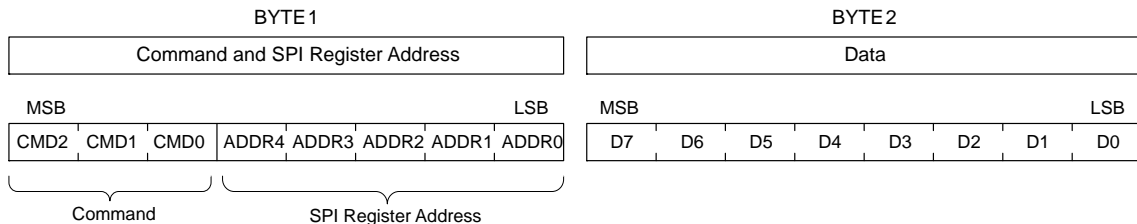


Figure 19. SPI Transfer Packet

Byte 1 contains the Command and the SPI Register Address and indicates to AMIS-30532 the chosen type of operation and addressed register. Byte 2 contains data, or

sent from the Master in a WRITE operation, or received from AMIS-30532 in a READ operation.

Two command types can be distinguished in the communication between master and AMIS-30532:

- READ from SPI Register with address ADDR[4:0]:
CMD2 = “0”
- WRITE to SPI Register with address ADDR[4:0]:
CMD2 = “1”

READ Operation

If the Master wants to read data from Status or Control Registers, it initiates the communication by sending a

READ command. This READ command contains the address of the SPI register to be read out. At the falling edge of the eight clock pulse the data-out shift register is updated with the content of the corresponding internal SPI register. In the next 8-bit clock pulse train this data is shifted out via DO pin. At the same time the data shifted in from DI (Master) should be interpreted as the following successive command or dummy data.

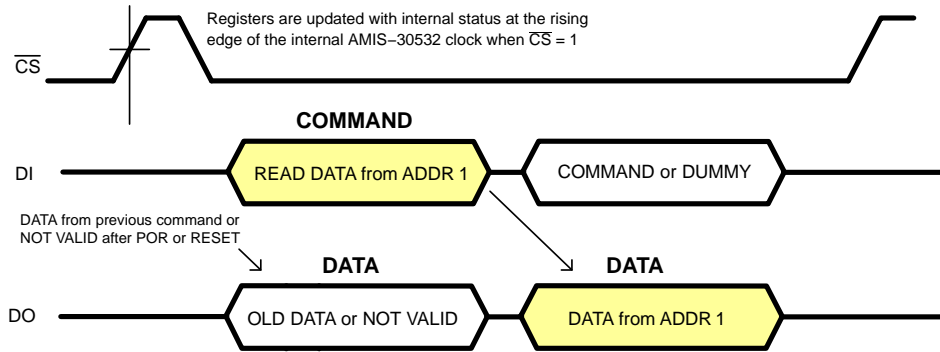


Figure 20. Single READ Operation where DATA from SPI register with Address 1 is read by the Master

All 4 Status Registers (see SPI Registers) contain 7 data bits and a parity check bit. The most significant bit (D7) represents a parity of D[6:0]. If the number of logical ones in D[6:0] is odd, the parity bit D7 equals “1”. If the number of logical ones in D[6:0] is even then the parity bit D7 equals “0”. This simple mechanism protects against noise and increases the consistency of the transmitted data. If a parity check error occurs it is recommended to initiate an additional READ command to obtain the status again.

Also the Control Registers can be read out following the same routine. Control Registers don’t have a parity check.

The \overline{CS} line is active low and may remain low between successive READ commands as illustrated in Figure 22. There is however one exception. In case an error condition is latched in one of Status Registers (see SPI Registers) the ERRB pin is activated. (See Section Error Output). This signal flags a problem to the external microcontroller. By reading the Status Registers information about the root cause of the problem can be determined. After this READ operation the Status Registers are cleared. Because the Status Registers and ERRB pin (see SPI Registers) are only updated by the internal system clock when the \overline{CS} line is

high, the Master should force \overline{CS} high immediately after the READ operation. For the same reason it is recommended to keep the \overline{CS} line high always when the SPI bus is idle.

WRITE Operation

If the Master wants to write data to a Control Register it initiates the communication by sending a WRITE command. This contains the address of the SPI register to write to. The command is followed with a data byte. This incoming data will be stored in the corresponding Control Register after \overline{CS} goes from low to high! AMIS-30532 responds on every incoming byte by shifting out via DO the data stored in the last received address.

It is important that the writing action (command – address and data) to the Control Register is exactly 16 bits long. If more or less bits are transmitted the complete transfer packet is ignored.

A WRITE command executed for a read-only register (e.g. Status Registers) will not affect the addressed register and the device operation.

Because after a power-on-reset the initial address is unknown the data shifted out via DO is not valid.

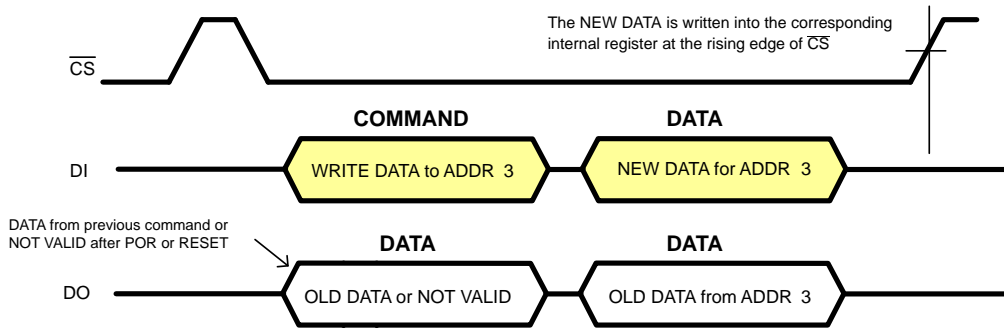


Figure 21. Single WRITE Operation where DATA from the Master is written in SPI register with Address 3

Examples of Combined READ and WRITE Operations

In the following examples successive READ and WRITE operations are combined. In Figure 22 the Master first reads the status from Register at ADDR4 and at ADDR5 followed

by writing a control byte in Control Register at ADDR2. Note that during the write command the old data of the pointed register is returned at the moment the new data is shifted in.

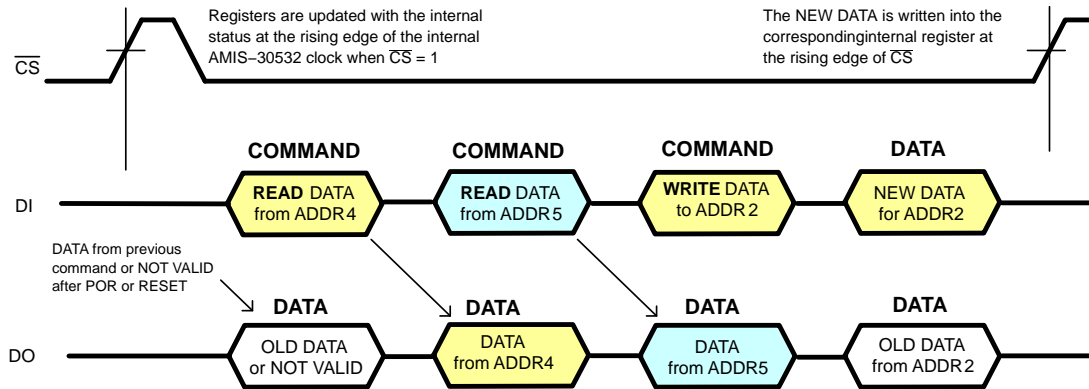


Figure 22. 2 Successive READ Commands Followed by a WRITE Command

After the write operation the Master could initiate a read back command in order to verify the data correctly written as illustrated in Figure 23. During reception of the READ command the old data is returned for a second time. Only after receiving the READ command the new data is

transmitted. This rule also applies when the master device wants to initiate an SPI transfer to read the Status Registers. Because the internal system clock updates the Status Registers only when \overline{CS} line is high, the first read out byte might represent old status information.

AMIS-30532

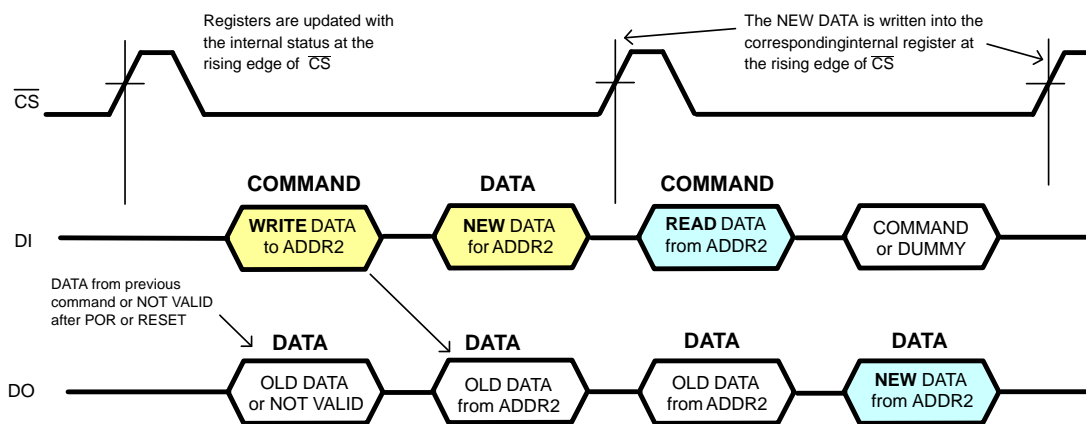


Figure 23. A WRITE Operation Where DATA from the Master is Written in SPI Register with Address 2 Followed by a READ Back Operation to Confirm a Correct WRITE Operation

NOTE: The internal data-out shift buffer of AMIS-30532 is updated with the content of the selected SPI register only at the last (every eight) falling edge of the CLK signal (see SPI Transfer Format and Pin Signals). As a result, new data for transmission cannot be written to the shift buffer at the beginning of the transfer packet and the first byte shifted out might represent old data.

Table 13. SPI CONTROL REGISTERS (All SPI control registers have Read/Write Access and default to “0” after power-on or hard reset)

| Address | Content | Structure | | | | | | | |
|-----------|---------|-----------|----------|-----------|----------|-------|-------|-----------|-------|
| | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| WR (00h) | Data | WDEN | WDT[3:0] | | | - | - | - | - |
| CR0 (01h) | Data | SM[2:0] | | | CUR[4:0] | | | | |
| CR1 (02h) | Data | DIRCTRL | NXTP | - | - | PWMF | PWMJ | EMC[1:0] | |
| CR2 (03h) | Data | MOTEN | SLP | SLAG | SLAT | - | - | - | - |
| CR2 (08h) | Data | M[1:0] | | StrB[1:0] | | - | StrC | StrE[1:0] | |

Where:

R/W: Read and Write access

Reset: Status after power-On or hard reset

Table 14. SPI CONTROL PARAMETER OVERVIEW

| Symbol | Description | Status | | Value |
|-----------|---|-------------|------------------------------|----------------------|
| DIRCTRL | Controls the direction of rotation (in combination with logic level on input DIR) | <DIR> = 0 | <DIRCTRL> = 0 | CW motion (Note 15) |
| | | | <DIRCTRL> = 1 | CCW motion (Note 15) |
| | | <DIR> = 1 | <DIRCTRL> = 0 | CCW motion (Note 15) |
| | | | <DIRCTRL> = 1 | CW motion (Note 15) |
| NXTP | Selects if NXT triggers on rising or falling edge | <NXTP> = 0 | Trigger on rising edge | |
| | | <NXTP> = 1 | Trigger on falling edge | |
| EMC[1:0] | Turn On – Turn-off Slopes of motor driver (Note 14) | 00 | Very Fast | |
| | | 01 | Fast | |
| | | 10 | Slow | |
| | | 11 | Very Slow | |
| SLAT | Speed load angle transparency bit | <SLAT> = 0 | SLA is transparent | |
| | | <SLAT> = 1 | SLA is NOT transparent | |
| SLAG | Speed load angle gain setting | <SLAG> = 0 | Gain = 0.5 | |
| | | <SLAG> = 1 | Gain = 0.25 | |
| PWMF | Enables doubling of the PWM frequency (Note 14) | <PWMF> = 0 | Default Frequency | |
| | | <PWMF> = 1 | Double Frequency | |
| PWMJ | Enables jittery PWM | <PWMJ> = 0 | Jitter disabled | |
| | | <PWMJ> = 1 | Jitter enabled | |
| SM[2:0] | Stepmode | 000 | 1/32 Micro – Step | |
| | | 001 | 1/16 Micro – Step | |
| | | 010 | 1/8 Micro – Step | |
| | | 011 | 1/4 Micro – Step | |
| | | 100 | Compensated Half Step | |
| | | 101 | Uncompensated Half Step | |
| | | 110 | Full Step | |
| | | 111 | n.a. | |
| SLP | Enables sleep mode | <SLP> = 0 | Active mode | |
| | | <SLP> = 1 | Sleep mode | |
| MOTEN | Activates the motor driver outputs | <MOTEN> = 0 | Drivers disabled | |
| | | <MOTEN> = 1 | Drivers enabled | |
| M[1:0] | PWM Mode Control | 00 | Default PWM control | |
| | | 01 | DCMin Mode 1 | |
| | | 10 | DCMin Mode 2 | |
| | | 11 | DCMin Mode 3 | |
| StrB[1:0] | PWM Strobe B Control: DON mask comparator time (Note 16) | 00 | 4 PWM clock cycles | |
| | | 01 | 8 PWM clock cycles | |
| | | 10 | 12 PWM clock cycles | |
| | | 11 | 19 PWM clock cycles | |
| StrC | PWM Strobe C Control: Switch time top/bottom regulation | <StrC> = 0 | 86% duty cycle PWM regulator | |
| | | <StrC> = 1 | 75% duty cycle PWM regulator | |
| StrE[1:0] | PWM Strobe E Control: Compensation bridge active time (Note 16) | 00 | 4 PWM clock cycles | |
| | | 01 | 8 PWM clock cycles | |
| | | 10 | 12 PWM clock cycles | |
| | | 11 | 19 PWM clock cycles | |

14. The typical values can be found in Table 5: DC Parameters and in Table 6: AC parameters

15. Depending on the wiring of the motor connections

16. The duration is depending on the selected PWM frequency

CUR[4:0] Selects IMCmax peak. This is the peak or amplitude of the regulated current waveform in the motor coils.

Table 15. SPI CONTROL PARAMETER OVERVIEW CUR[4:0]

| Current Range (Note 18) | Index CUR[4:0] | | Current (mA) (Note 17) | Current Range (Note 18) | Index CUR[4:0] | | Current (mA) (Note 17) |
|----------------------------|-------------------|-------|---------------------------|----------------------------|-------------------|-------|---------------------------|
| 0 | 0 | 00000 | 66 | 2 | 16 | 10000 | 735 |
| | 1 | 00001 | 135 | | 17 | 10001 | 800 |
| | 2 | 00010 | 189 | | 18 | 10010 | 883 |
| | 3 | 00011 | 200 | | 19 | 10011 | 975 |
| | 4 | 00100 | 221 | | 20 | 10100 | 1077 |
| | 5 | 00101 | 244 | | 21 | 10101 | 1189 |
| | 6 | 00110 | 269 | | 22 | 10110 | 1255 |
| | 7 | 00111 | 297 | | 23 | 10111 | 1485 |
| 1 | 8 | 01000 | 328 | 3 | 24 | 11000 | 1625 |
| | 9 | 01001 | 366 | | 25 | 11001 | 1767 |
| | 10 | 01010 | 400 | | 26 | 11010 | 1950 |
| | 11 | 01011 | 442 | | 27 | 11011 | 2153 |
| | 12 | 01100 | 488 | | 28 | 11100 | 2378 |
| | 13 | 01101 | 538 | | 29 | 11101 | 2552 |
| | 14 | 01110 | 594 | | 30 | 11110 | 2775 |
| | 15 | 01111 | 654 | | 31 | 11111 | 3015 |

17. Typical current amplitude at T_J = 125°C

18. Reducing the current over different current ranges might trigger overcurrent detection. See dedicated application note for solutions

SPI Status Register Description

All 4 SPI status registers have Read Access and are default to "0" after power-on or hard reset.

Table 16. SPI STATUS REGISTERS

| Address | Content | Structure | | | | | | | |
|------------------|---------------------|-----------|----------|--------|---------|--------|-------|-------|-------|
| | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | Access | R | R | R | R | R | R | R |
| SR0 (04h) | Data is not latched | PAR | TW | CPfail | WD | OPENX | OPENY | - | - |
| SR1 (05h) | Data is latched | PAR | OVCXPT | OVCXPB | OVCXNT | OVCXNB | - | - | - |
| SR2 (06h) | Data is latched | PAR | OVCYPT | OVCYPB | OVCYYNT | OVCYNB | TSD | - | - |
| SR3 (07h) | Data is not latched | PAR | MSP[6:0] | | | | | | |

Where:

- R Read only mode access
- Reset Status after power-on or hard reset
- PAR Parity check

Table 17. SPI STATUS FLAGS OVERVIEW

| Mnemonic | Flag | Length (bit) | Related SPI Register | Comment | Reset State |
|----------|--|--------------|--------------------------|---|-------------|
| CPFail | Charge pump failure | 1 | <u>Status Register 0</u> | '0' = no failure '1' = failure: indicates that the charge pump does not reach the required voltage level. Note 1 | '0' |
| MSP[6:0] | Micro-step position | 7 | <u>Status Register 3</u> | Translator micro step position | '0000000' |
| OPENX | OPEN Coil X | 1 | <u>Status Register 0</u> | '1' = Open coil detected | '0' |
| OPENY | OPEN Coil Y | 1 | <u>Status Register 0</u> | '1' = Open coil detected | '0' |
| OVCXNB | O Ver Current on X H-bridge; MOTXN terminal; B ottom tran. | 1 | <u>Status Register 1</u> | '0' = no failure '1' = failure: indicates that over current is detected at bottom transistor XN-terminal | '0' |
| OVCXNT | O Ver Current on X H-bridge; MOTXN terminal; T op transist. | 1 | <u>Status Register 1</u> | '0' = no failure '1' = failure: indicates that over current is detected at top transistor XN-terminal | '0' |
| OVCXPB | O Ver Current on X H-bridge; MOTXP terminal; B ottom tran. | 1 | <u>Status Register 1</u> | '0' = no failure '1' = failure: indicates that over current is detected at bottom transistor XP-terminal | '0' |
| OVCXPT | O Ver Current on X H-bridge; MOTXP terminal; T op transist. | 1 | <u>Status Register 1</u> | '0' = no failure '1' = failure: indicates that over current is detected at top transistor XP-terminal | '0' |
| OVCYNB | O Ver Current on Y H-bridge; MOTYN terminal; B ottom tran. | 1 | <u>Status Register 2</u> | '0' = no failure '1' = failure: indicates that over current is detected at bottom transistor YN-terminal | '0' |
| OVCYNT | O Ver Current on Y H-bridge; MOTYN terminal; T op transist. | 1 | <u>Status Register 2</u> | '0' = no failure '1' = failure: indicates that over current is detected at top transistor YN-terminal | '0' |
| OVCYPB | O Ver Current on Y H-bridge; MOTYP terminal; B ottom tran. | 1 | <u>Status Register 2</u> | '0' = no failure '1' = failure: indicates that over current is detected at bottom transistor YP-terminal | '0' |
| OVCYPT | O Ver Current on Y H-bridge; MOTYP terminal; T op transist. | 1 | <u>Status Register 2</u> | '0' = no failure '1' = failure: indicates that over current is detected at top transistor YP-terminal | '0' |
| TSD | Thermal shutdown | 1 | <u>Status Register 2</u> | | '0' |
| TW | Thermal warning | 1 | <u>Status Register 0</u> | | '0' |
| WD | Watchdog event | 1 | <u>Status Register 0</u> | '1' = watchdog reset after time-out | '0' |

NOTE: WD – This bit indicates that the watchdog timer has not been cleared properly. If the master reads that WD is set to “1” after reset, it means that a watchdog reset occurred (warm boot) instead of POR (cold boot). WD bit will be cleared only when the master writes “0” to WDEN bit.

Table 18. ORDERING INFORMATION

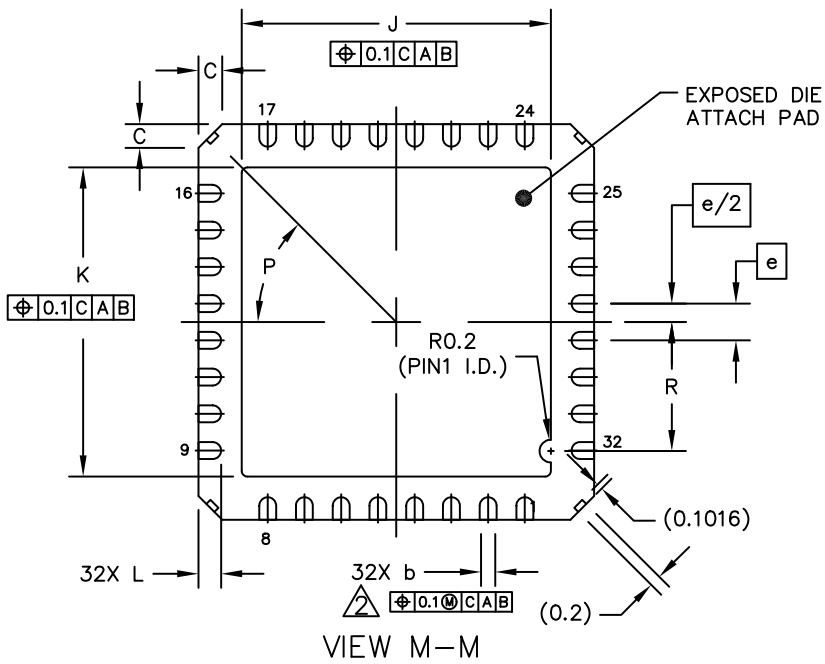
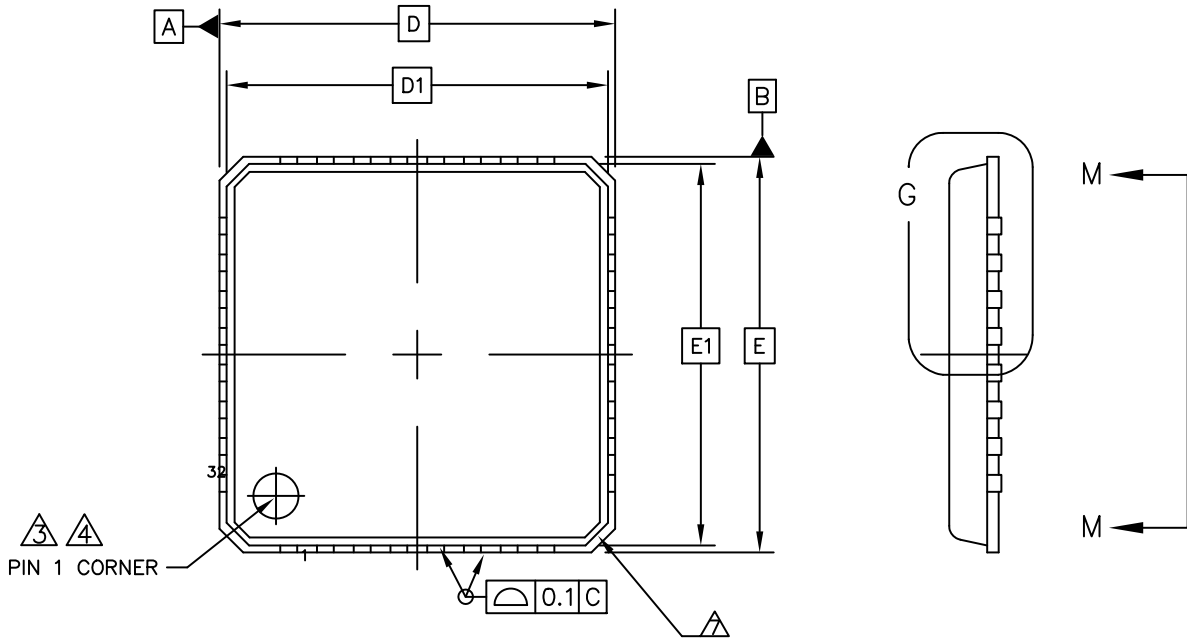
| Part No. | Peak Current | Temperature Range | Package | Shipping† |
|------------------|--------------|-------------------|---------------------------------|-------------|
| AMIS30532C5321RG | 1600 mA | -40°C to 125°C | NQFP-32 (7 x 7 mm) (Pb-Free) | Tape & Reel |
| AMIS30532C5321G | 1600 mA | -40°C to 125°C | NQFP-32 (7 x 7 mm) (Pb-Free) | Tube |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

AMIS-30532

PACKAGE DIMENSIONS

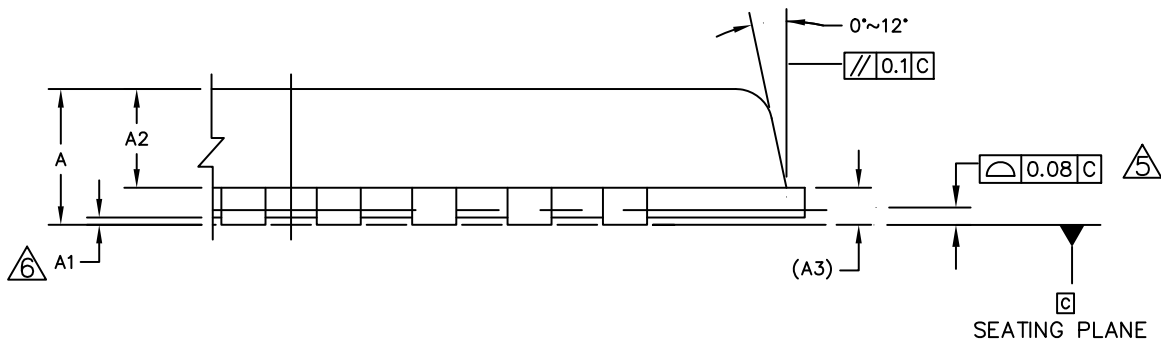
NQFP-32, 7x7
CASE 560AA
ISSUE O



AMIS-30532

PACKAGE DIMENSIONS

NQFP-32, 7x7
CASE 560AA
ISSUE O



DETAIL G
VIEW ROTATED 90° CLOCKWISE

| DIM | MIN | NOM | MAX | NOTES |
|-----|-------|------------|--------------------------|---|
| A | 0.8 | | 0.9 | 1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM) △ DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP. △ THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY. △ EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL. △ APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING. △ APPLIED ONLY TO TERMINALS. △ EXACT SHAPE OF EACH CORNER IS OPTIONAL. |
| A1 | 0 | 0.02 | 0.05 | |
| A2 | 0.576 | 0.615 | 0.654 | |
| A3 | | 0.203 REF. | | |
| b | 0.25 | 0.3 | 0.35 | |
| C | 0.24 | 0.42 | 0.6 | |
| D | | 7 BSC | | |
| D1 | | 6.75 BSC | | |
| E | | 7 BSC | | |
| E1 | | 6.75 BSC | | |
| e | | 0.65 BSC | | |
| J | 5.37 | 5.47 | 5.57 | |
| K | 5.37 | 5.47 | 5.57 | |
| L | 0.35 | 0.4 | 0.45 | |
| P | | 45° REF | | |
| R | 2.185 | | 2.385 | |
| | | UNIT | DIMENSION AND TOLERANCES | |
| | | MM | ASME_Y14.5M | JEDEC-MO-220_REV.F |

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